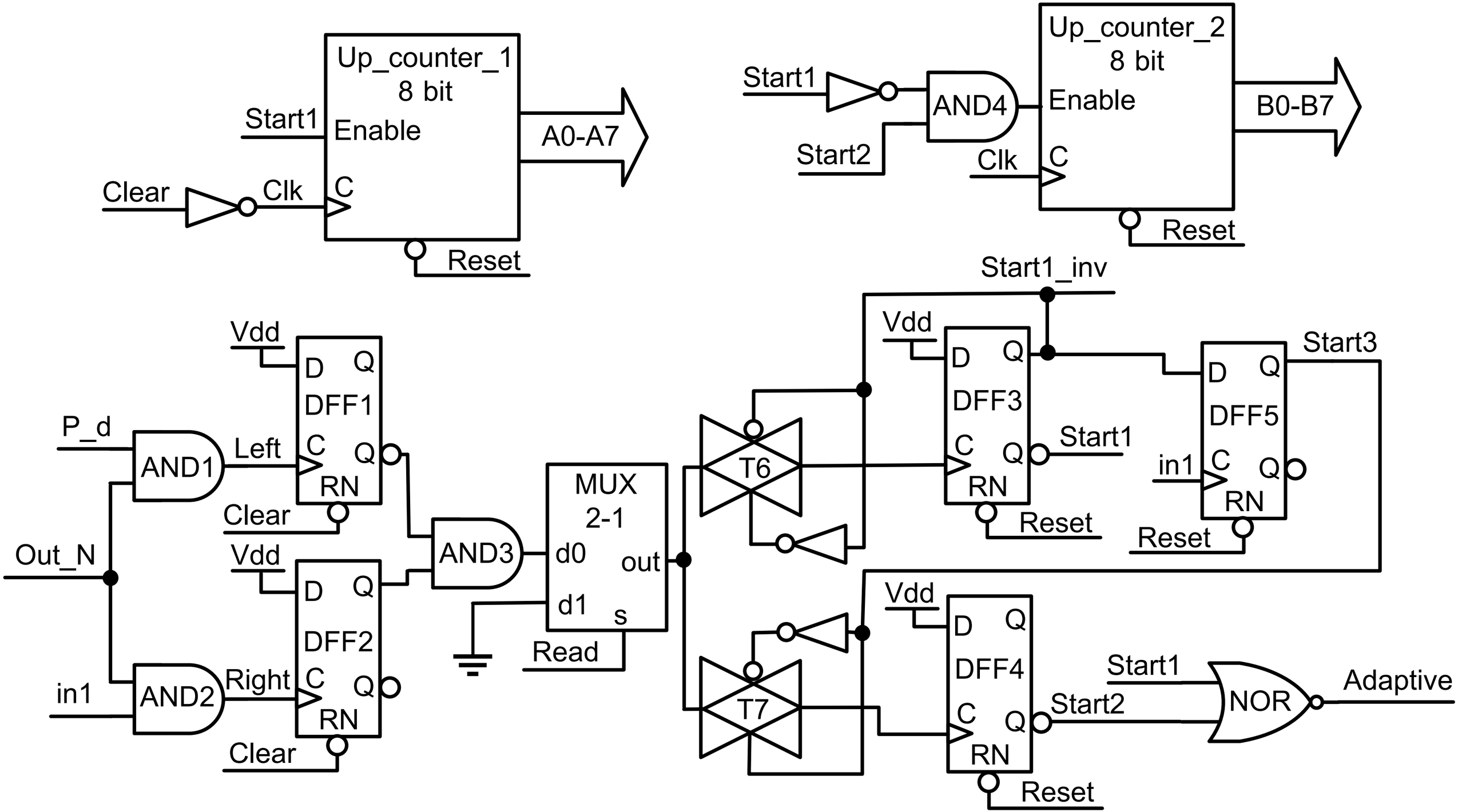
Up_counter_1
8 bit
Start1
Enable
A0-A7
Clear
Clk
C
Reset
Up_counter_2
8 bit
Start1
AND4
Enable
B0-B7
Start2
Clk
C
Reset
Start1_inv
Vdd
D
Q
DFF1
P_d
AND1
Left
C
Q
RN
Clear
Out_N
Vdd
D
Q
DFF2
AND3
MUX
2-1
d0
out
d1
s
Read
in1
AND2
Right
C
Q
RN
Clear
T6
T7
Vdd
D
Q
DFF3
C
Q
Start1
RN
Reset
Start3
D
Q
DFF5
in1
C
Q
RN
Reset
Vdd
D
Q
DFF4
C
Q
RN
Reset
Start1
Start2
NOR
Adaptive