



Automated contactless characterization of local thin film thickness and film stress with standard MEMS structures at wafer level

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Abstract. The fabrication of microelectromechanical systems (MEMS) devices comprises many steps, each of which adds to the tolerance, resulting in device performances that may fall outside the defined limits in the design process. Hence, it is important to know local thin film properties most accurately, directly affecting the performance of the MEMS device. Furthermore, the capability of monitoring and mapping the thin film thickness and stress across a wafer enables device statistics and the strengthening of scientific statements. Within this study, we used standard MEMS structures consisting of a cantilever and a step profile to perform automated and contactless characterization of the local thin film thickness and stress across six 4-inch (100 mm) wafers. For this purpose, we constructed a measurement setup combining white light interferometry (WLI) to measure the static deflection of the cantilevered beams and plates and the thickness of the thin film through a step profile etched into the thin film. Even more, an *XYZ*-stage positions hundreds of devices below the objective lens of the WLI. This leads to precise maps of the local thin film thickness and to the extraction of a mean stress and a gradient stress from the static deflection of slender beams. The beams are oriented parallel and perpendicular to the wafer flat so that the measurement of orientation-dependent stress values is possible.

1 Introduction

Microelectromechanical systems (MEMS) have progressed from research prototypes to a pervasive technology platform underpinning both high-end industrial applications and widely adopted consumer products. Their presence across domains such as automotive, medical diagnostics, mobile electronics, and precision instrumentation (Bhatt et al., 2019; Chircov and Grumezescu, 2022; Kurmendra and Kumar, 2021; Khoshnoud and Silva, 2012) illustrates the degree to which MEMS have become fully established in modern electronic-based systems. In this context, device statistics serve as a rigorous framework for benchmarking performance within specific device concepts, enabling systematic evaluation of design, reliability, and functional efficiency. Independent of the application field, standard device architectures in MEMS require the integration of one or more thin

films to achieve the targeted functionality. The thin films are either grown on the substrate or bonded to the substrate, resulting in a stacked material system at wafer level with two or more layers of different materials, including interfaces. Due to these challenging batch-compatible thin film fabrication processes and subsequent micromachining for the MEMS device fabrication, any tolerances from each fabrication step add up, which may result in output performance parameters out of the acceptable limits. Over the past 30 years, the MEMS industry has relied on statistical metrology to gain insights into individual device variations, both at wafer level and throughout entire fabrication batches, as described by Boning and Chung (1996). However, only a limited number of publications have so far discussed statistical approaches. Recently, this topic was addressed for resonantly operated MEMS (Kurth et al., 2007; Gennat et al., 2013; Huber et al., 2025b), where, in the latter study, hundreds of pure

single-crystalline silicon cantilevered resonators were evaluated with respect to mode-dependent resonance frequencies and quality factors.

For resonating devices, local change of the film stress and also the thin film thickness affect the properties of the MEMS devices and make precise local monitoring of these parameters necessary even during the fabrication of MEMS devices. However, the local film stress is influenced by several contributions in material stacks (Huff, 2022), like different lattice parameters and coefficients of thermal expansion (CTE) (Moll et al., 2025). The crystallinity of the layer – whether amorphous, polycrystalline, or single-crystalline – further influences stress. In single crystals, it may stem from doping or point defects, whereas in polycrystalline films it is linked to growth processes and grain boundary formation (Chason and Guduru, 2016). Techniques like physical vapor deposition (PVD) or magnetron sputtering can strongly modify stress due to the bombardment with energetic particles, not only affecting the surface of the thin film but also penetrating into the surface-near bulk region of the material, so that the crystal lattice gets surface-near distorted or gas atoms from the plasma atmosphere get trapped in the film (Abadias et al., 2018).

Many techniques have been developed to measure the film stress at wafer level or locally at a specific position. Different approaches are classified by Chen and Ou (2015) into (1) techniques measuring wafer curvature, (2) material-level nondestructive measurements, (3) specimens and structure characterization techniques, and (4) material-level destructive measurements.

1. While the measurement of the curvature can be performed either at wafer level (mainly with capacitive techniques) or on smaller snippets (mainly with optical techniques), Stoney's equation is used in most cases to calculate the stress (Stoney and Parsons, 1909). Therefore, the thicknesses of the device layer and substrate need to be known, but a local variation in the parameters cannot be taken into account, and only an averaged stress value across the sample is calculated. However, since curvature measurements are fast and easy to implement in the fabrication process of MEMS devices, they are widespread in industry and academia (Brouzet et al., 2019).
2. The second class summarizes X-ray diffraction (XRD) techniques and Raman spectroscopy. X-ray and Raman techniques are based on the measurement of lattice spacings in crystalline materials, and, with the knowledge of elastic properties, the stress can be calculated from a generalized Hook's law. XRD either measures several diffraction peaks with conventional laboratory XRD systems (Genzel et al., 2012) or nanodiffraction using synchrotron facilities (Keckes et al., 2012). The nanodiffraction techniques are able to achieve local stress depth profiles and therefore allow scanning mate-

rial stacks and interfaces. The study by De Wolf (1996) describes how Raman spectroscopy can be used to measure phase shifts in Raman peaks in correlation to the present stress in a silicon integrated circuit due to a change of the lattice parameter.

3. Within the third class of techniques, standard fabrication processes are used to pattern the thin film of interest and fabricate simple MEMS structures, e.g., microbeams, and subsequently analyze the static deflection. This is done mainly with scanning electron microscopy (SEM) (Guckel et al., 1992) or interferometry, including white light interferometry (WLI) (Cuthrell et al., 1988; Lober et al., 1988; Conor et al., 2003; Bosseboeuf and Petitgrand, 2003), but capacitive approaches are also reported (Osterberg and Senturia, 1997). A comparison of different devices, including strain-gauge structures, is done by Masters et al. (2001). Another technique is the bulge test method. It was established in the 1950s, and the accuracy has increased since then (see Small and Nix, 1992). It can be used to determine material properties of thin films by measuring the deflection of a membrane due to a pressure applied to one side of the membrane (Chen and Ou, 2015).
4. Finally, in the fourth class, focused ion beam (FIB)-based methods are reported frequently, combining the controlled FIB milling of structures on the film with SEM and digital image correlation (Valente et al., 2005). With this advanced technique, the local stress can again be monitored as a function of milling depth, and good agreement with XRD methods is demonstrated (Abadias et al., 2018).

Available stress measurement techniques, however, are typically limited to specific components of the stress tensor. In particular, XRD and FIB milling are advanced techniques compared to others and are time- and cost-intensive. Moreover, absolute stress values obtained from different methods are often difficult to compare, since the measurement principles impose limitations such as averaging over volumes and crystallographic directions. This also prevents the application of otherwise useful models, for example, the approximation of uniaxial residual stress as the superposition of a constant mean stress and a gradient stress demonstrated by Fang and Wickert (1996). WLI, by contrast, offers a fast and versatile approach that can be readily applied to a broad range of quality inspection tasks, such as surface characterization (Baryshev et al., 2013) or the analysis of effects in micro-machined beams (Jensen et al., 1999). In this work, WLI is employed as an optical profiling technique to determine both the local device layer thickness, via scans of trenches in the device layer in the area of the silicon frame, and the static deflection of cantilevers with different orientations on the wafer, thereby enabling the extraction of orientation-dependent residual stress values.

The present study describes a passive MEMS structure to simultaneously measure the local device layer thickness and the orientation-dependent static deflection of a cantilever. An automated contactless WLI setup is constructed and used to scan hundreds of devices fabricated on different single- and polycrystalline device layers of 4-inch (100 mm) wafers. Considerations on stress in a bent beam enable the calculation of local stress values from the measurement of the actual device layer thickness and static deflection of the cantilever and when knowing the Young's modulus and Poisson's ratio, respectively. By doing so, we are able to obtain for each device individually the information on thickness and the uniaxial deflection, hence the local uniaxial residual stress as a superposition of a mean stress and a gradient stress.

2 Stress in a bent beam

The residual stress in a thin film can be expressed in general form via the stress tensor σ :

$$\sigma = \begin{pmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{pmatrix}. \quad (1)$$

Within the study of slender beams, we focus on the uniaxial residual stress along the beam axis, leading to the beam's deformation. Hence, the total uniaxial residual stress deforming the slender beam is represented by the polynomial

$$\sigma_{\text{uniaxial}} = \sum_{k=0}^{\infty} \sigma_k \left(\frac{z}{h/2} \right)^k, \quad (2)$$

where h is the thickness of the beam and z is the coordinate across the thickness with the zero point in the midplane of the beam. Following the argumentation of Fang and Wickert (1996), we consider the constant mean stress σ_0 and the gradient stress σ_1 only. They can be attributed to a mismatch of the thermal expansion coefficient between the thin film and substrate and to local effects, including graining (e.g., size and distribution) and structural defects in the thin film, respectively. This leads to the simplified form of the uniaxial stress:

$$\sigma_{\text{uniaxial}} = \sigma_0 + \sigma_1 \frac{z}{h/2}. \quad (3)$$

The first term subsumes symmetric stress components, and the latter one represents anti-symmetric components. Furthermore, following the work of Fang and Wickert (1996), the distinction between tilt and curl deformations is introduced, related to the mean and the gradient stress, respectively. They approximate the deflection shape of the beam with a quadratic function:

$$z(x) \approx (\theta_0 + \theta_1)x + \frac{1}{2R}x^2, \quad (4)$$

where x is the coordinate along the beam axis, R is the constant radius of the curvature, and θ_0 and θ_1 are the total angular rotation of the thin film at the anchor. Fang and Wickert (1996) calculate θ_0 and θ_1 via a finite element method (FEM) as

$$\begin{aligned} \theta_0 &\approx \frac{\sigma_0}{E} (1.33 + 0.45\nu)(-0.014h + 1.022) \\ \theta_1 &\approx \frac{\sigma_1}{E} (0.0086h^2 - 0.047h + 0.81), \end{aligned} \quad (5)$$

where E and ν are the Young's modulus and the Poisson's ratio of the thin film, respectively. Additionally, σ_1 is indirectly proportional to R , as $\sigma_1 = Eh/2R$.

The separation into tilt and curl is illustrated in Fig. 1. In Fig. 1a and b, the mean stress σ_0 is negative, equal to a downwards tilt. The superposition of a negative gradient stress further curls the beam down, as shown in Fig. 1a. In Fig. 1b, the superposition with positive σ_1 results in a positive value of the 500 μm long cantilever for the deflection at the tip $z(x = 500 \mu\text{m})$, already for $\sigma_1 = 10 \text{ MPa}$, which is 2 orders of magnitude lower than the absolute value of σ_0 . In Fig. 1c and d, σ_0 is positive; hence the tilt points upwards. Again, the superposition with σ_1 leads to an additional curl in the corresponding direction. In Fig. 1c, similarly to Fig. 1b, a gradient stress 2 orders of magnitude smaller than the mean stress is able to change the sign of the static deflection at the tip of the cantilever. In conclusion, it can be stated that the amplitude of the static deflection depends much more on σ_1 than on σ_0 . This behavior of the static deflection can also be seen in Eq. (4), where σ_1 contributes to both the linear and the quadratic term, while σ_0 only affects the linear term.

3 Experimental details

Different silicon, 3C-SiC, and diamond device layers with various thicknesses, microstructures, and mechanical properties are investigated on phosphorus-doped (100)-oriented silicon substrates covered with a wet thermal oxide, summarized in Table 1. The deposition of polycrystalline 3C-SiC is performed in an LPCVD system. An alternating supply deposition (ASD) working with alternating gas flows of propane and silane with intermediate pump-out times is utilized, as described in Moll et al. (2024). Polycrystalline diamond (PCD) thin films from CarbonCompetence GmbH are fabricated in an HFCVD system at elevated temperatures from methane and hydrogen as precursor gases. For deposition of the PCD films with grains of several micrometers in diameter (m-PCD) and PCD films with small grains in the range of several nanometers (n-PCD), the temperature of the Si substrate was set to 800–850 °C and a total gas pressure of 5 mbar was applied, while the filament-to-substrate distance was maintained at 50 mm. The applied gas flows for the deposition of m-PCD and n-PCD films are set to CH_4/H_2 ratios of 0.1% and 2%, respectively. Further details on the deposition parameters can be found in Meindlhumer et al.

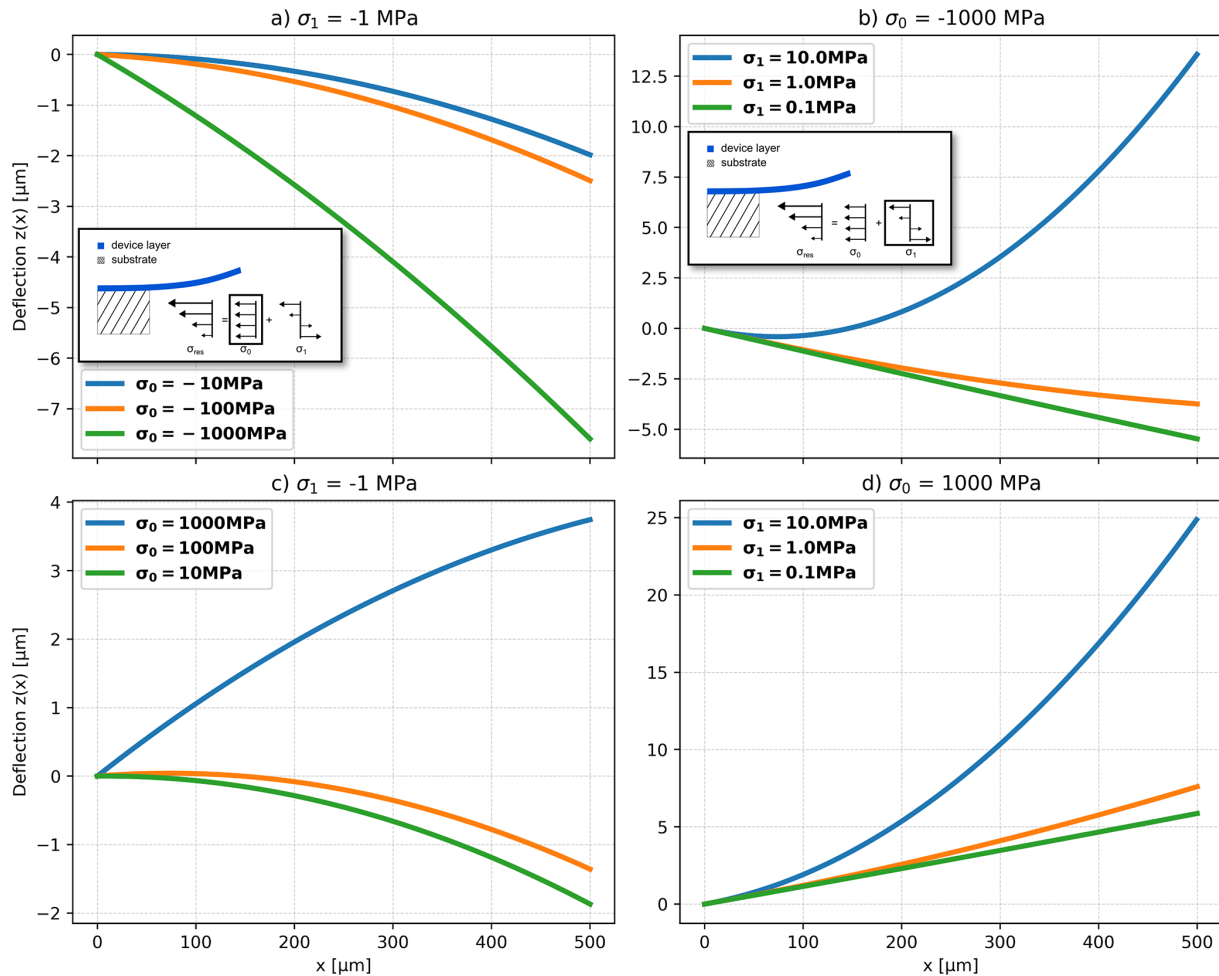


Figure 1. Theoretically predicted tilt and curl deformations of a beam with $h = 1$ μm, $E = 130$ GPa, and $\nu = 0.25$.

(2024) and Huber et al. (2024). The grown thin films are benchmarked with single-crystalline silicon (SCSi) from a commercially available SOI wafer and with polycrystalline silicon (PCSi), as these are standard materials for MEMS devices. Two depositions of PCSi in an LPVCD system are performed at different temperatures, leading to very small nano-sized silicon grains (s-PCSi) at a deposition temperature of 568 °C and larger grains by 2 orders of magnitude (l-PCSi) at a deposition temperature of 600 °C.

A Bosch process is used for micromachining single- and polycrystalline silicon. Furthermore, we developed suitable dry-etching recipes for PCSiC and PCD in a capacitively coupled plasma (CCP), STS RIE, and in an inductively coupled plasma reactive ion etcher (ICP RIE), Oxford Plasmalab 100, summarized in Table 2. We achieved an etching rate up to 100 nm min⁻¹ for PCD and up to 150 nm min⁻¹ for PCSiC, while for the selected etching parameters, the etch rate depends on the grain size of the polycrystalline device layer.

Test structures consisting of a cantilever and a step profile (SP) close to the anchor region are presented in Fig. 2a. The SP consists of 50 μm wide trenches etched through the device layer, down to the buried oxide. By utilizing the Bosch process, the cantilevers are released from the substrate, whereas the stress in the device layer leads to a static deflection. Cantilevers with a constant length of 500 μm and a width of 50 μm were fabricated to characterize the local stress distribution.

A Micro System Analyzer (MSA-400) from Polytec GmbH, equipped with a 10 times magnifying Mirau objective and a piezoelectrically actuated stage, is used for static device characterization. An automated measurement setup is constructed to scan many devices fabricated on the same wafer at different positions for analyzing device layer thickness and film stress with WLI. To position the wafer below the objective, three motorized linear stages from Zaber Technologies Inc. are used both for the in-plane positioning and to focus on each device. A horizontal x -stage (X-LSM100A), a horizontal y -stage (X-LSM150A), and a vertical z -stage (X-

Table 1. Investigated device layers.

Device layer	n-PCD	m-PCD	l-PCSi	s-PCSi	SCSi	3C-SiC
Details	Nanometer-sized grains	Micrometer-sized grains	Large grains ≈ 100 nm	Small grains several nm	Single-crystalline	Polycrystalline, Moll et al. (2024)

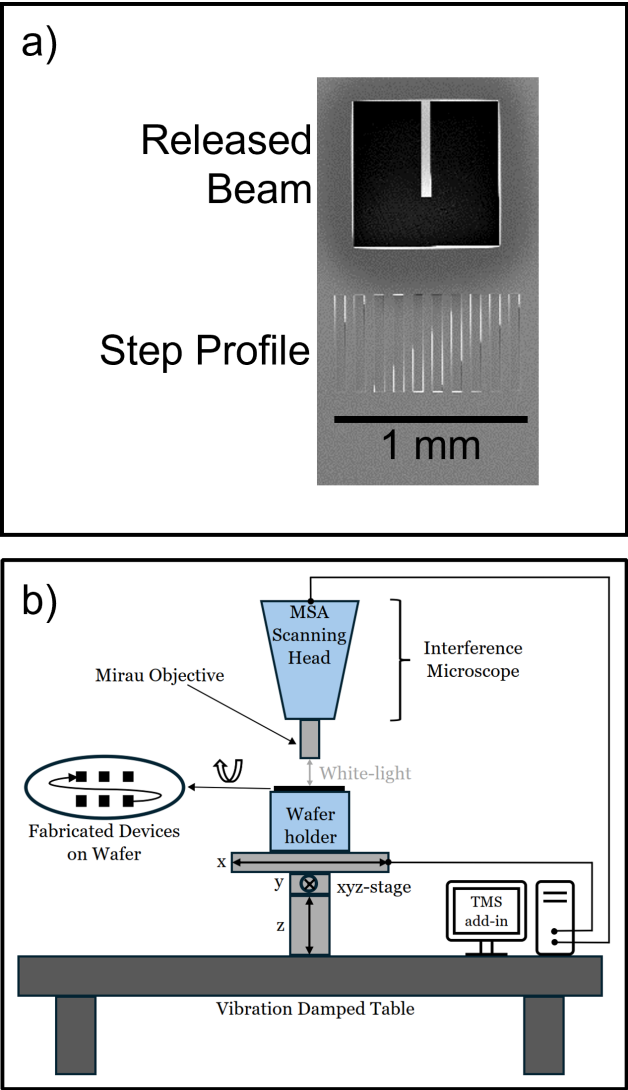


Figure 2. (a) The automated contactless characterization of the local thin film thickness and stress uses a standard MEMS test structure with a cantilever and a step profile. (b) The WLI measurement setup consists of an MSA-400 equipped with a Mirau objective and an XYZ-stage.

Table 2. Etch recipe for PCSiC and PCD.

Material	RIE	Parameter	Value
PCSiC	CCP	Temperature	25 °C
		RF generator power	300 W
		SF ₆ gas flow	5 sccm
		O ₂ gas flow	25 sccm
		Chamber pressure	150 mTorr
PCD	ICP	Temperature	25 °C
		ICP power	1000 W
		RF generator power	100 W
		O ₂ gas flow	49 sccm
		CHF ₃ gas flow	0–1 sccm (cycles of 1 min)
		Chamber pressure	15 mTorr

VSR20A) with travel ranges of 100, 150, and 20 mm, respectively, are mounted on a vibration-damped table. Further on, each position stage, along with the MSA-400, is controlled with the same script to ensure an automated scan of all the devices at wafer level. A schematic representation of the measurement setup is shown in Fig. 2b.

From the three-dimensional scan of the SP, we extract an averaged profile line perpendicular to the etch trenches with several edges after the frontside etch, as shown in Fig. 3 for l-PCSi. In advance, leveling is performed, such that the upper plateaus of the SP are leveled out and set to 0. Even more, the leveling ensures that the maximum trench depth can be extracted accurately from the measurement data. A spatial step function z_{step} is designed to cover the specific shape of the trenches with rounded corners resulting from the dry-etching process:

$$z_{\text{step}} = z_0 + A \tanh(s \cos(2\pi f x + \phi)).$$

(6)

The parameter s in Eq. (6) has the default settings $s_u = 10$ if $\cos(2\pi f x + \phi) > 0$ and $s_l = 4$ for the sharpness of the upper and lower edges, respectively. Additionally, f is the fixed spatial frequency of the trenches, z_0 is the offset in height, and ϕ is the offset in the in-plane direction. Both the device layer thickness and the device height are determined as twice the amplitude A . The measurement is benchmarked with a stylus profilometer measurement, and very similar results are found. A similar approach is used for the extraction of the static deflection from the WLI scan of the cantilever. The plane correction is again done to minimize any impact from a tilted sample position, and the static deflection $z(x)$ is fitted with Eq. (4). A representative measurement and fitting procedure is shown in Fig. 4, again for l-PCSi.

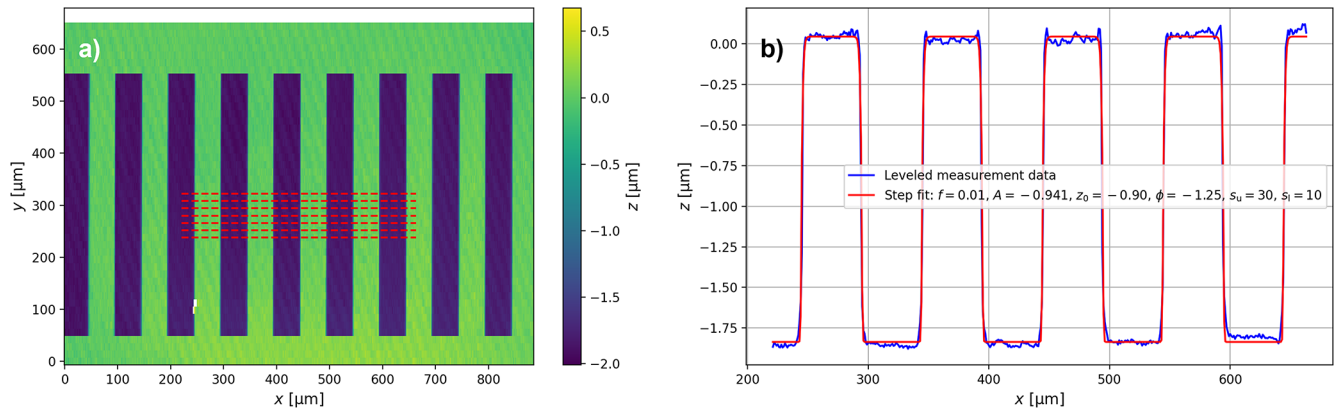


Figure 3. (a) Typical leveled topography measurement of the step profile (SP) etched into the l-PCSi thin film. (b) Fit of Eq. (6) to the extracted average center line of the topography measurement.

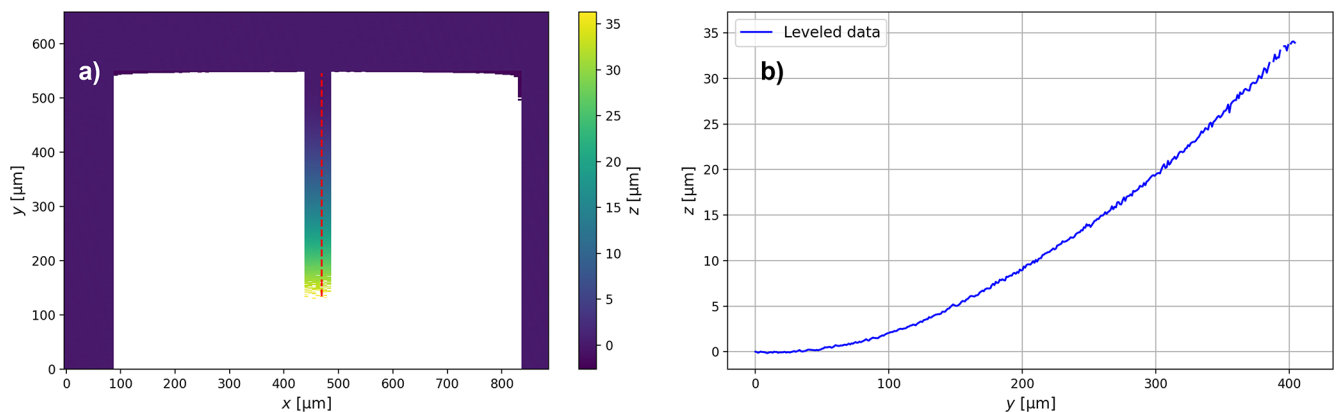


Figure 4. (a) Typical leveled topography measurement of a l-PCSi beam. (b) Extracted deflection curve of the beam from the topography measurement.

Finally, we performed measurements of the wafer curvature with the l-PCSi, s-PCSi, and n-PCD thin films using an MX203-6-33 Wafer Geometry Gauge from E+H Metrology GmbH.

4 Results

The material properties needed for the fitting procedures of the model by Fang and Wickert (1996) to the measured deflection curves of the cantilevers are summarized in Table 3. Standard values for SCSi are used from Hopcroft et al. (2010), while the Young's modulus of s-PCSi, l-PCSi, and PCSiC is calculated from the EB theory, the measured resonance frequency of the first EB mode, and the measured device layer thickness. We show the calculated stress distribution of the polycrystalline silicon device layer with small grains in the nanometer range (s-PCSi) for 40 devices with a length of 500 μm and a width of 50 μm in Fig. 5. The cantilever devices in each lower row are oriented parallel to the wafer flat, while the cantilever devices in each upper row are oriented perpendicular to the flat. Since the stress might not

be isotropic, this approach allows us to distinguish between the stress values in two different directions (σ_{\perp} and σ_{\parallel}) in close vicinity to minimize the impact of other parasitic effects, such as from microstructural variations. Results shown in the upper part of Fig. 5 represent the calculated mean stress σ_0 . We find compressive stress in most of the parallel devices and tensile stress in the perpendicular devices, with a huge difference in their mean values ($\bar{\sigma}_{0,\parallel}$ and $\bar{\sigma}_{0,\perp}$) of about 1542 MPa. However, the lower part of Fig. 5 shows the calculated gradient stresses in both directions and gives their mean values across the wafer in parallel and perpendicular directions, $\bar{\sigma}_{1,\parallel}$ and $\bar{\sigma}_{1,\perp}$, respectively. For the gradient stresses, we find negative, hence compressive, stress all over the wafer and a rather small difference in the mean values from parallel to perpendicular devices of about 24 MPa.

We performed the same study of 40 devices for each of five different thin films (SCSi, s-PCSi, l-PCSi, n-PCD, and PCSiC) with WLI and the model from Fang and Wickert (1996) and summarized the results in Fig. 6. The data of the m-PCD film, however, were too noisy for WLI characterization, due to the rough surface of the device layer. The

Table 3. Young’s modulus E and Poisson’s ratio ν of the thin films studied.

Device layer	E (GPa)	ν
n-PCD	460 (Meindlhumer et al., 2024)	0.06 (Klein and Cardinale, 1993)
l-PCSi	103	0.25 (Hopcroft et al., 2010)
s-PCSi	97	0.25 (Hopcroft et al., 2010)
SCSi	130 (Hopcroft et al., 2010)	0.25 (Hopcroft et al., 2010)
PCSiC	226 (Huber et al., 2025a)	0.19 (Jackson, 2005)

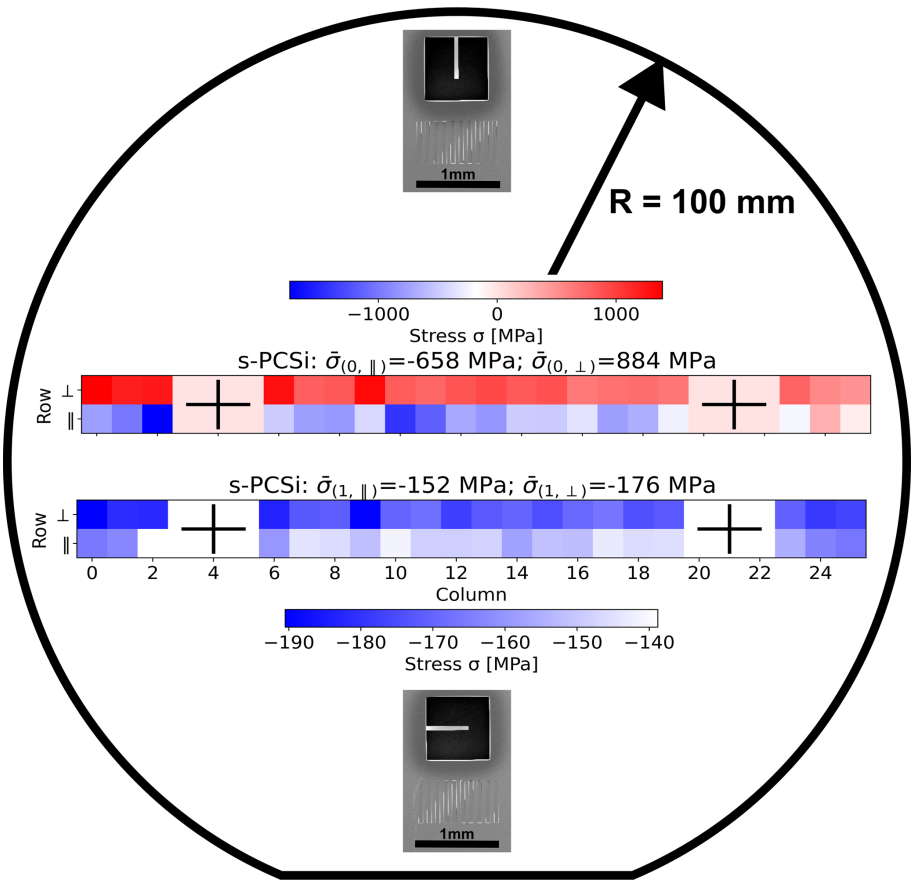


Figure 5. Beams oriented parallel and perpendicular to the wafer flat are arranged in rows of 20 devices across the 4-inch (100 mm) wafer. For the presented data of s-PCSi, the local thickness is measured with the step profile (SP) and used to determine the mean stresses $\sigma_{0,\parallel}$ and $\sigma_{0,\perp}$ (in the upper part of the figure) and the gradient stresses $\sigma_{1,\parallel}$ and $\sigma_{1,\perp}$ (in the lower part of the figure). While for the gradient stresses all devices show negative (compressive) stresses, most of the devices parallel to the flat show negative mean stress, but all devices perpendicular to the flat show positive (tensile) $\sigma_{0,\perp}$.

data are plotted per device, while every fit of the beam’s deflection accounts for the local thickness of the device layer extracted from the measurement of the step profile. Furthermore, the data are separated into parallel and perpendicular devices and into gradient and mean stress. When focusing on the mean stress σ_0 representing the tilt of the beams, we find a low tensile mean stress of 67 MPa in SCSi. A tensile but very high σ_0 of 1650 MPa is also measured for PCSiC for both directions. Moderate absolute values of mean stress up to absolute values of 500 MPa can be found for n-PCD but

by changing the sign from negative (compressive) to positive (tensile) from parallel to perpendicular. Similar behavior is present in l-PCSi (σ_0 -absolute values up to 600 MPa). A much larger change can be found for s-PCSi (σ_0 -absolute values up to 1700 MPa), as shown in Fig. 5. We find a very consistent trend for all device layers for σ_1 , independent of the orientation of the test structure. Since the thickness of the device layer changes from the center to the edge of the wafer, symmetric changes of σ_1 can be found for n-PCD and PCSiC, while the silicon device layers show rather constant

values. In particular, the SCSi device layer does not show any curl of the beams, resulting in $\sigma_1 = 0$.

A WLI measurement on a single device takes about 40 s, including the postprocessing steps. Repeated measurements are performed on the same device with ResonatorID = 182 on the l-PCSi wafer for 24 h. The gradient stress averaged for 210 measurements is calculated as $\sigma_1 = 40.95 \pm 1.47$ MPa.

5 Discussion

The direction-dependent mean stress σ_0 measured for the polycrystalline silicon device layer with large grains in the range of ≈ 100 nm (l-PCSi), the polycrystalline silicon device layer with small grains in the nanometer range (s-PCSi), and the polycrystalline diamond device layer with small grains in the nanometer range (n-PCD) can be caused by several parameters during the deposition. Non-uniform temperatures in the CVD process, along with asymmetric gas flows, can lead to an anisotropic stress distribution in the wafer. Furthermore, the CTE is highly temperature-dependent, and even for SCSi and PCSi, the parameters differ by roughly a factor of 2 for different temperatures, as described by Mazur and Gasik (2009) for SCSi and by Tada et al. (2000) for PCSi-SiO₂ stacks. The CTE is also dependent on the crystal orientation of the thin film, especially for SCSi, but also for PCSi, if there is a preferred growth direction. However, the identification of the microstructural origin of the direction-dependent stress is outside the scope of this work. Furthermore, the fitting procedure due to the leveling within the applied method is critical for the extraction of the correct mean stress, and the results shown for σ_0 need to be used carefully, since small measurement and fitting uncertainties have a huge impact on σ_0 . A schematic is shown in Fig. 7, where the angle α represents the leveling error. The angle θ is the tilt of the beam at the anchor and is calculated as the sum of θ_0 and θ_1 . Since θ_1 is fixed by σ_1 and the measured radius of the curvature R in Eq. (5), the leveling error in a measurement is directly added to θ_0 and hence to σ_0 . An uncertainty of the leveling resulting in a device tilt $\alpha = 1$ mrad for a 2 μ m thick beam leads to a variation in σ_0 of 90.7 and 341 MPa for SCSi and n-PCD, respectively.

The calculation of the local device layer stress is done with precise knowledge of the thickness at each position. The presented structures are used to characterize six thin films with WLI. Hence, 182 devices fabricated on half of a 4-inch (100 mm) wafer are fully automatically measured to extract the local thickness and static deflection information. With this information, it is possible to map the local properties, as shown for the thickness in Fig. 8. The maps show different distributions of the device layer depending on whether its thickness is locally either thinner or thicker. Wafer bonding, as done for the fabrication of the single-crystalline silicon device layer within an SOI process, leads to a pattern originating from the subsequent grinding process to define the thin

film thickness. The other device layers fabricated from CVD are showing more random patterns related to the gas flow in the CVD reactor and the relative positions of the gas inlets. However, we find the standard deviation of the thickness to be minimal for the PCSi wafers used, medium for the SCSi and the m-PCD device layers, and maximal for the n-PCD thin film, respectively. Regions of the PCSiC device layer were destroyed during device fabrication; hence, no thickness map is shown for this thin film.

As already mentioned, the extraction of σ_1 from the measured curvature of the cantilevers leads to a symmetric result for parallel and perpendicular devices. For the gradient stress, the influence of the device tilt is irrelevant, and a closer look at the effect of the local thin film thickness on σ_1 is done in Fig. 9. To do so, we calculated the average thin film thickness \bar{h} for the 40 studied devices per device layer and show the difference between the gradient stress calculated with the local thin film thickness h_{loc} and the one with \bar{h} per device in both directions, parallel and perpendicular to the wafer flat. While the difference is below 10 MPa in most of the measurements, it reaches up to 38 MPa for PCSiC at the edge of the wafer, indicating the high precision of the presented combination of film thickness and film stress measurement.

Stoney's equation, widely used to calculate the effective mean stress $\bar{\sigma}$ of a film from wafer curvature measurement techniques, is very convenient since it needs the thin film thickness h as the only thin film input parameter:

$$\bar{\sigma} = \frac{E_S}{1 - \nu_S} \frac{h_S^2}{6hR}. \quad (7)$$

The radius R is measured optically or capacitively, and the properties of the substrate E_S , ν_S , and h_S (the Young's modulus, the Poisson ratio, and the thickness, respectively) are known. From considerations of the total force per unit width acting on the edge of the wafer f by Chason and Guduru (2016), one finds an expression for the so-called stress thickness $\bar{\sigma}h$

$$f = \bar{\sigma}h = \int_{-h/2}^{h/2} \sigma_{uniaxial} dz + f_{Surface} + f_{Interface}, \quad (8)$$

where $f_{Surface}$ and $f_{Interface}$ are additional forces related to the surface of the thin film and the interface between substrate and thin film. Expressing the effective mean stress from Eq. (8) and inserting Eq. (3) leads to $\bar{\sigma}$ depending only on the mean stress of the thin film, since the integral cancels out the stress gradient symmetric around the midplane of the thin film. Hence, it is clear that curvature measurements are only capable of measuring stress related to the mean stress in a thin film but cannot give any information on the gradient stress.

However, for the static deflection of MEMS devices, it is crucial to know both components to the residual stress. The

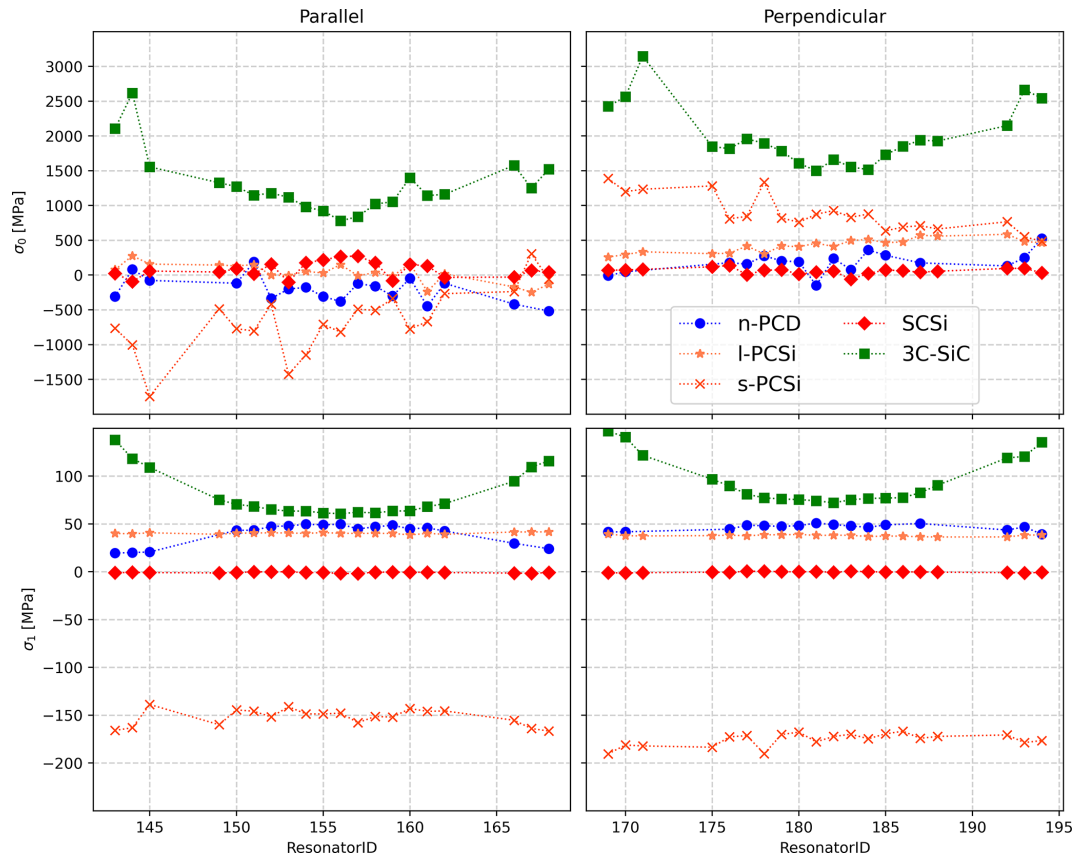


Figure 6. The mean stress (in the upper half) and the gradient stress (in the lower half) are shown for parallel- and perpendicular-oriented devices, relative to the wafer flat. A total of 20 devices for each orientation are measured with a length of 500 μm and a width of 50 μm . While σ_1 does not show any orientation dependence, the mean component of the stress changes from parallel to perpendicular for n-PCD, I-PCSi, and s-PCSi. The inserted lines serve as a visual guide.

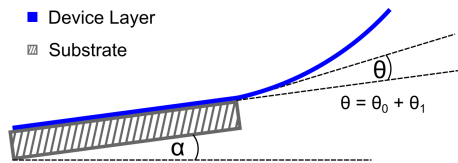


Figure 7. Schematic representation of the impact of a device tilt α on the measured tilt of the beam at the anchor θ .

list of three different MEMS cantilevers fabricated from I-PCSi, s-PCSi, and n-PCD in Fig. 10 compares the visible static deflection from the SEM image with the measured values of the effective mean stress from a capacitive wafer bow (WB) measurement and the mean values of $\bar{\sigma}_0$ and $\bar{\sigma}_1$ across 40 devices on each wafer, as described for Fig. 6. The I-PCSi cantilever shows an upwards static deflection, while the stress value from WB is negative. This discrepancy can be overcome by taking the positive $\bar{\sigma}_1$ into account. A situation like this is demonstrated in Fig. 1b, where the negative slope at the anchor and the superposition of the positive curl deflection lead to an overall positive deflection at the tip of the

cantilever. Unfortunately, the measured $\bar{\sigma}_0$ value for this thin film does not fit the WB result due to possible limitations in the leveling procedure, also discussed above. Nevertheless, great accordance is found in the stress measurements for s-PCSi. For s-PCSi, the WB and the WLI values for $\bar{\sigma}_0$ are 115 and 113 MPa, while the averaged $\bar{\sigma}_1$ gives -164 MPa. These results describe a situation as shown in Fig. 1c. The static deflection of the s-PCSi cantilever shows a downwards bending with a rather high amplitude, as shown in the SEM image in Fig. 10. Finally, the n-PCD cantilever shows vanishing stress in the WB of 1 MPa, even though there is a slight static deflection visible in the SEM image of Fig. 10. The detailed analysis of the devices with WLI gives a rather high $\bar{\sigma}_1 = 43$ MPa, resulting from the small curvature and the high value of diamond's Young's modulus.

Further validation of the presented method is needed, since the gradient stress cannot be confirmed with wafer bow measurements. Possible alternatives to validate the results of this study are more elaborate techniques, like cross-sectional nanodiffraction XRD measurements (Keckes et al., 2012) or focused ion beam (FIB)-based methods. In the latter technique, a deformation analysis of a microstructure after sequential

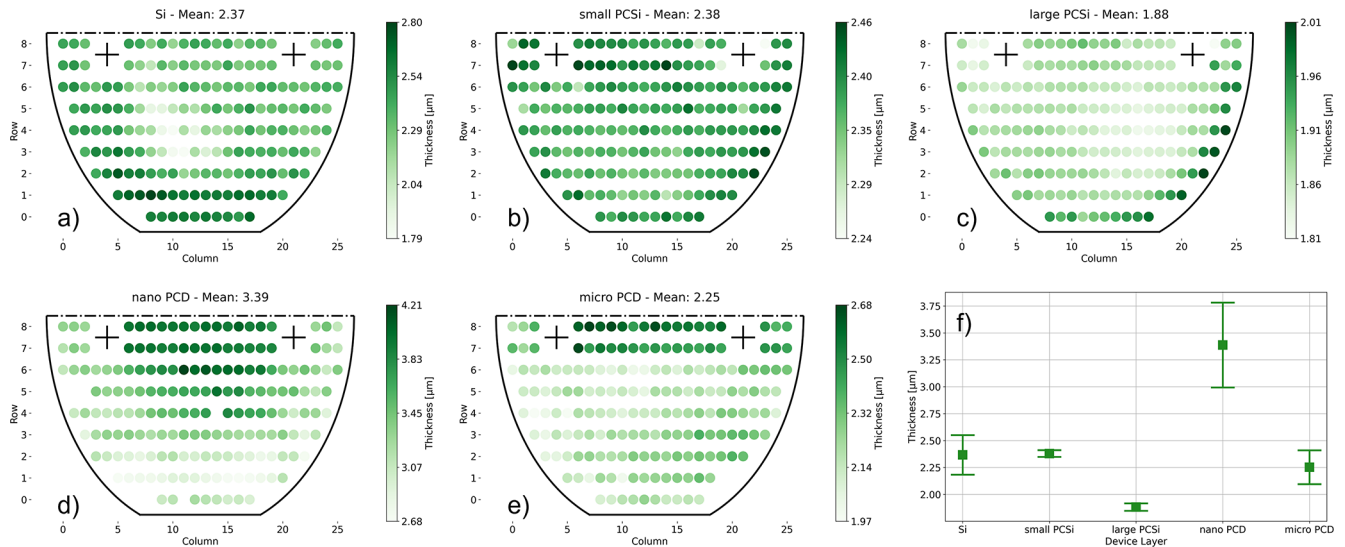


Figure 8. Maps of 182 measurement points on half of a 4-inch (100 mm) wafer for (a) SCSi, (b) s-PCSi, (c) l-PCSi, (d) n-PCD, and (e) m-PCD. Their mean values and standard deviations are shown in panel (f).

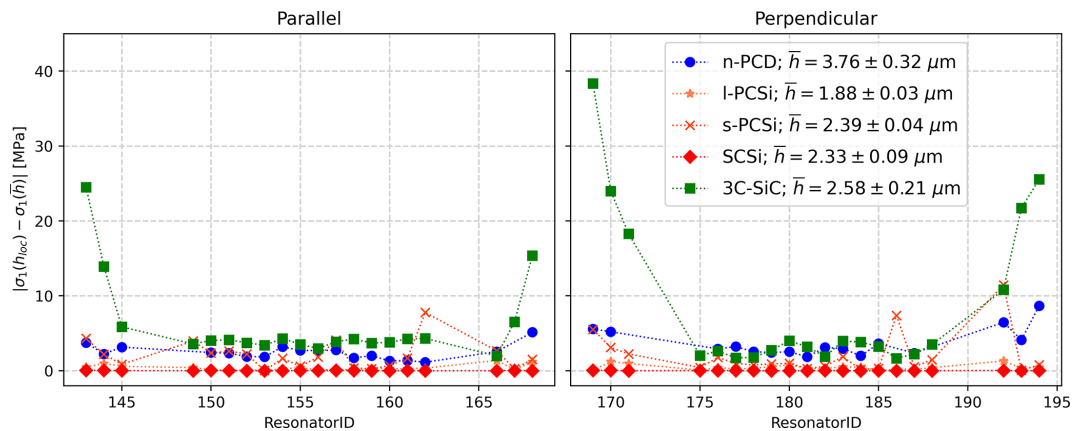


Figure 9. Calculated differences between σ_1 measured with the accurate local thin film thickness h_{loc} and σ_1 calculated with an averaged thickness \bar{h} .

FIB-milling steps provides depth information on the stress in the studied film and hence the present stress gradient (Valente et al., 2005).

6 Conclusions and outlook

We present an MEMS test structure that is straightforward to fabricate with standard techniques of the MEMS industry in combination with an automated WLI measurement setup to determine local thin film thickness and film stress. The test structures are applied to six different device layers, revealing different thickness and static deflection distributions across the wafers. We calculate the local uniaxial mean stress σ_0 and gradient stress σ_1 following the FEM approach by Fang and Wickert (1996). This calculation is done by dividing the deflection into a tilt and curl component and performing a

fit of a quadratic function to the extracted deflection curve. By scanning devices across the wafer automatically, we get stress and thickness values at different positions on the wafer and with the orientation of the cantilever parallel and perpendicular to the wafer flat. We find local variation in the stress due to the device layer deposition processes and demonstrate that for polycrystalline silicon and diamond device layers, an orientation dependence of the stress is present. Furthermore, we want to highlight the impact of the gradient stress on the curl deflection of the devices, resulting in large deflection amplitudes often hidden by measurements of the average residual stress with curvature measurement techniques. These findings illustrate the need for a detailed knowledge of the thin film properties for the fabrication of MEMS devices, as stress in the device layer affects the fabricated MEMS device in several ways.

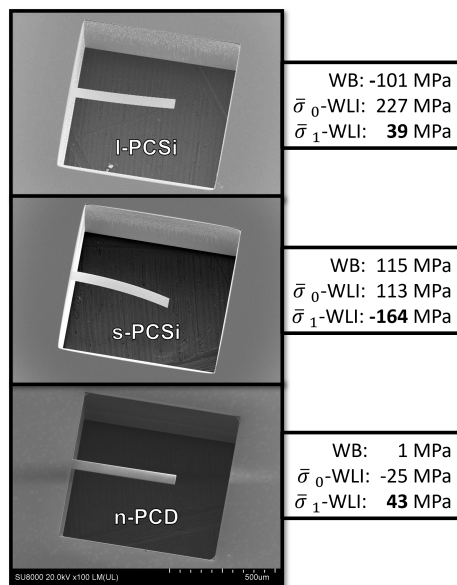


Figure 10. SEM images of representative cantilevers from the l-PCSi, s-PCSi, and n-PCD thin films with the measured stress values from wafer bow (WB) and WLI techniques.

As demonstrated, WLI can provide information, static deflection, and thickness in a contactless, fast, and automated way; hence, this technique can be used in both academia and industry for stress inspection. The precision of the measured mean stress can be further improved by scans of larger regions supported by the silicon frame, leading to a more effective leveling of the device. Furthermore, the approach by Fachin et al. (2011), combining WLI scans of single-side clamped cantilevers and double-side clamped bridges, is promising. The study of bridges allows the extraction of a parameter related to the clamping properties to distinguish between simply supported and fixed clamped bridges. However, the measurement of bridges is not capable of measuring tensile stresses, since no static deflection is present. Hence, the combined study of bridges and cantilevers overcomes the problem of leveling, since supported areas of the device on both ends of the bridges can be used, and additional information on the clamping properties can lead to an even higher precision of the measurement.

Code availability. The computer code used is available on request from the corresponding author.

Data availability. The data that support the findings of this study are available from the corresponding author upon reasonable request.

Author contributions. The conceptualization of the paper was done by DH, GP, and US. DH prepared the original draft, while GP and US did the supervision. CS built the software together with DH and AG. GP acquired the funding for the project and did the administration. Infrastructure and other resources were contributed by DS and US. Finally, investigations and visualizations were performed by DH and CS.

Competing interests. At least one of the (co-)authors is a member of the editorial board of *Journal of Sensors and Sensor Systems*. The peer-review process was guided by an independent editor, and the authors also have no other competing interests to declare.

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