



Investigation of low-temperature cofired ceramics packages for high-temperature SAW sensors

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Abstract. Surface acoustic wave (SAW) temperature sensor devices have been developed for operating temperatures up to and above 1000 °C. A challenging task to make these devices available on the market is to develop an appropriate housing concept. A concept based on low-temperature cofired ceramics (LTCC) has been investigated and tested under elevated temperatures up to 600 °C. The devices showed promising results up to 450 °C. Thorough analysis of the possible failure mechanisms was done to increase the maximum temperature above this limit in further production cycles.

1 Introduction

As surface acoustic wave (SAW) devices are widely spread as frequency filters and resonators for frequencies above 100 MHz, sensing applications are distributed in niche fields where silicon-based sensors cannot be applied. For wireless temperature measurements, SAW sensors have been shown to be capable to withstand temperatures up to and above 1000 °C, but with bare crystals without housing. For easy handling and to protect the crystal, housing is needed. As packaging materials, two main families can be identified: metal housings with glass or glass-ceramic wire feedthrough for signal routing and ceramic housings with filled vias and contact pads. In this paper, the latter types will be examined in a first approach to verify if the whole assembly concept is feasible. Low-temperature cofired ceramics (LTCC) allows for integration of embedded antenna structures on the outside of the housing, so this material has additional advantages over metal housings, which always need to be contacted to an antenna structure for radio frequency (RF) interrogation and tend to become leaky or break at the feedthrough. As test device, a reflective SAW delay line on Langasite (LGS) with aluminum–platinum (Al–Pt) based metallization is chosen due to its robustness (Bardong, 2013).

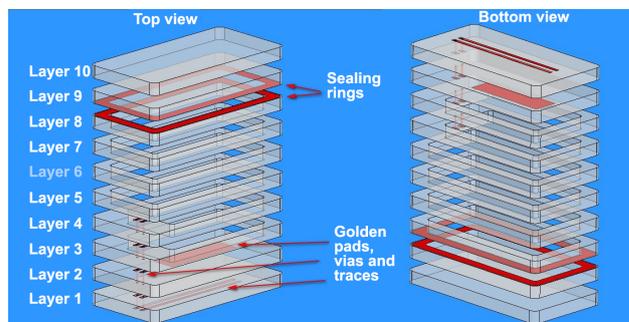


Figure 1. 3-D model of LTCC housing: top and bottom view, split up in the described layers.

2 Materials and methods

LTCC technology offers versatile structuring of complex channels and cavities within a single ceramic layer due to its possibility for selection of various tapes with different thicknesses and physical characteristics. This technology is suitable for applications in harsh and corrosive environments due to excellent hermeticity as well as thermal and chemical resistance of ceramic material.

The designed LTCC housing is made out of several tape layers. Some carry vias for signal routing, some are gold

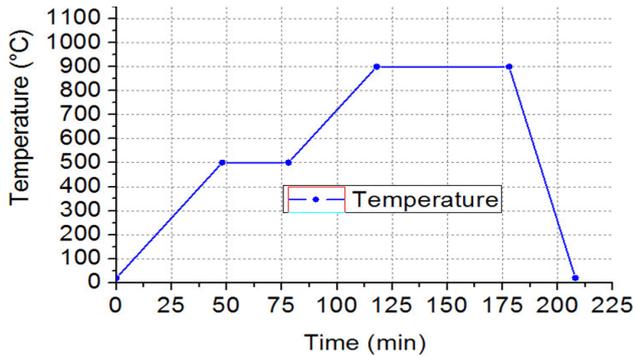


Figure 2. Sintering phase 1: Two-step sintering profile of LTCC CeramTec GC tape.



Figure 3. Fabricated housings after two-step sintering profile of LTCC CeramTec GC tape: top view.

plated via screen printing (Fig. 1). The top layer has a glass sealing ring on it to apply the lid.

The total outer dimensions of the housing are $7 \times 13.8 \times 2.4 \text{ mm}^3$ for width, length, and height, respectively. The structuring is done in the green state of the material by an Nd:YAG laser.

For this housing, the standardized process to develop 3-D structures with cavities has to be modified to achieve defect-free devices; as the cavities are quite large, making a defect-free lamination during the isostatic pressing process is a challenging task.

The LTCC housing is fabricated using commercially available CeramTec GC LTCC tape. This tape shows pronounced reliability and stability in high-temperature environments (Toskov et al., 2013). Commercially available and compatible ESL 8881 gold conductive paste has been selected to screen print the conductive pads and traces and ESL 8835 VF gold conductive paste for the via filling. The drying process of the gold conductive pastes was carried out at 125°C for 15 min. Due to the large cavity in layers 3, 4, and 5–8, the

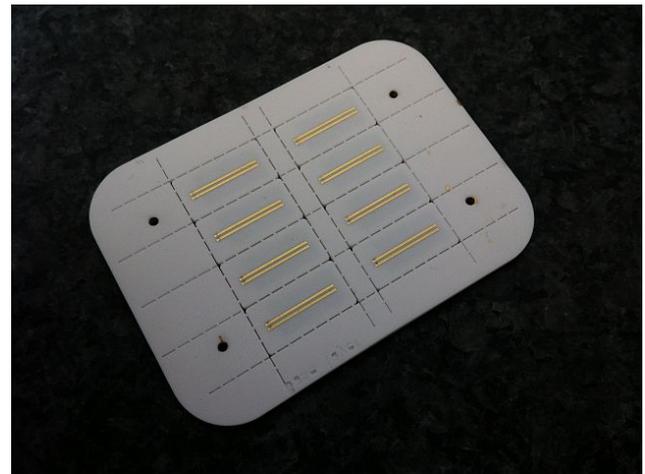


Figure 4. Fabricated housings after two-step sintering profile of LTCC CeramTec GC tape: bottom view.

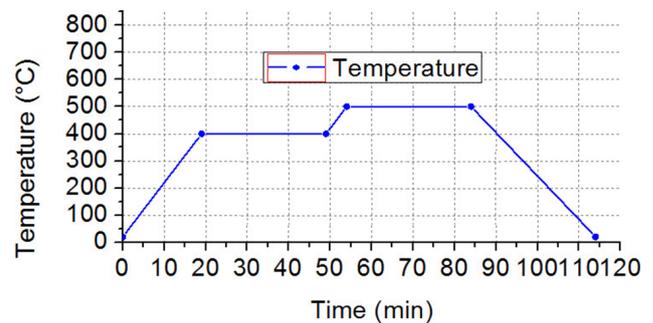


Figure 5. Sintering phase 2: Two-step ESL 4031-B glass sealing paste burn off and sintering.

lamination process has been executed in four separate steps. In the first three steps, layers 1–2, 3–4, and 5–8 were laminated to ensure lamination integrity of each of these parts, respectively. In each step, single ceramic layers were centred and stacked together in a steel compression mold and thermally compressed in a uniaxial press for 3.5 min, at 75°C , and a pressure of 64 bar. The final step was dedicated to the lamination of all the previously laminated subgroups.

The sintering process was carried out in three separate phases devoted to: (1) LTCC sintering in a Linn box furnace (Fig. 2), (2) burn off and sintering of screen-printed glass sealing rings, and (3) finally sealing of the entire LTCC housing after chip mounting and wire bonding.

Fabricated structures after the first sintering phase are presented in Figs. 3 and 4.

Right after the first sintering phase, the glass seals were screen printed at the top of the eighth layer stack and the bottom side of the lid (layer 9). Figure 5 shows the corresponding heat treatment profile to burn out organic compounds of the paste. In Fig. 6, the housing parts after these steps are presented.

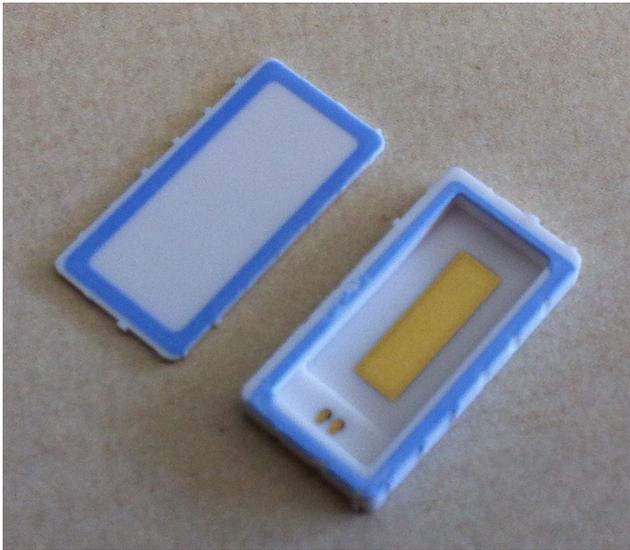


Figure 6. Fabricated LTCC housing after ESL 4031-B glass sealing paste burn off and sintering.

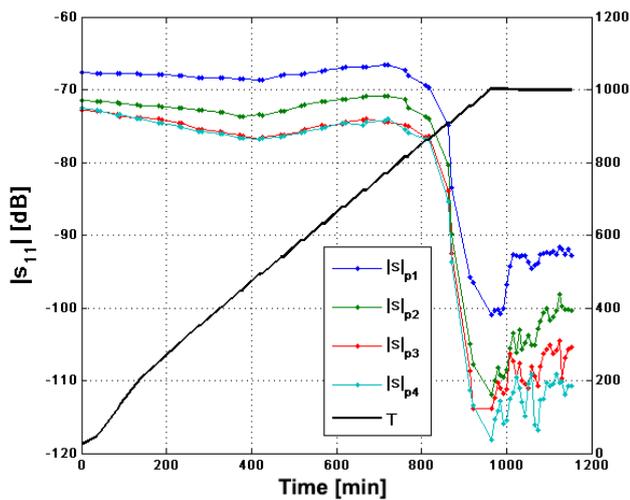


Figure 7. Bare device impulse amplitudes during annealing up to 1000 °C in Argon. The black line indicates the linear temperature rise and corresponds with the abscissa at the right. The device readings are stable up to 850 °C.

For the test, Langasite reflective delay lines with a Pt–Al stack of 105 nm thickness were chosen to be mounted into the housing (da Cunha et al., 2007; Bardong et al., 2010). The dies alone showed signals up to 900 °C (Fig. 7) (Bardong, 2013).

Therefore, the dies were placed on a dispensed amount of nanosilver paste and sintered onto the gold area inside the housing. Sintering was performed at 280 °C for 40 min on a hotplate.

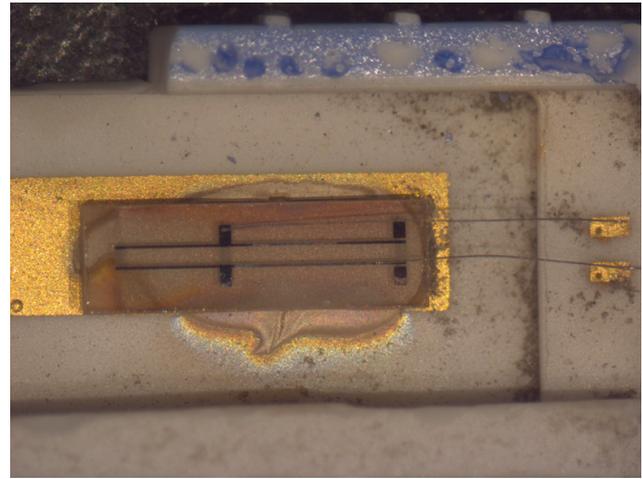


Figure 8. Reopened LTCC housing after heat treatment. Langasite crystal, contacting wire bonds, and nanosilver paste can be identified. Residual grinding dust from the opening process is visible between crystal and bonding pads of the LTCC.

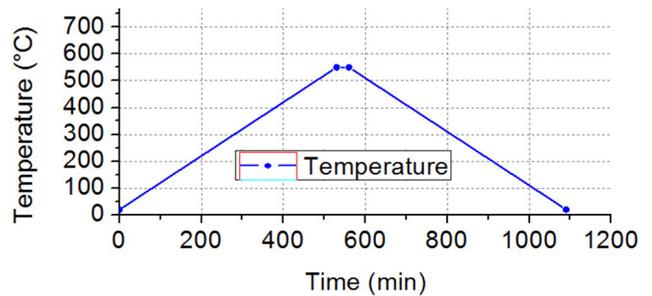


Figure 9. Temperature profile for the ESL 4031-B sealing paste with Langasite SAW sensor inside the housing.

To establish electrical contacts, the dies were bonded with Pt wires to the feed-through gold pads. In Fig. 8, a reopened setup is shown after heat treatment.

Finally, the lid was closed using a slow heating and cooling rate to avoid thermally induced stress (Fig. 9).

The closed devices were contacted and fixed in place with several platinum wires to a device carrier (Fig. 10), which was then mounted into a sample holder described in Bardong et al. (2009) and processed under the temperature setting described in the following part of this text. The atmosphere was set to 1 hPa of nitrogen in a tube furnace.

3 Measurements and signal processing

For heat treatment, the furnace was programmed to hold temperature levels from 250 to 600 °C in steps of 50 K. To get a first impression about the long-term stability of the housed device, each temperature level was kept for 20 h with an RF interrogation cycle every 15 min.

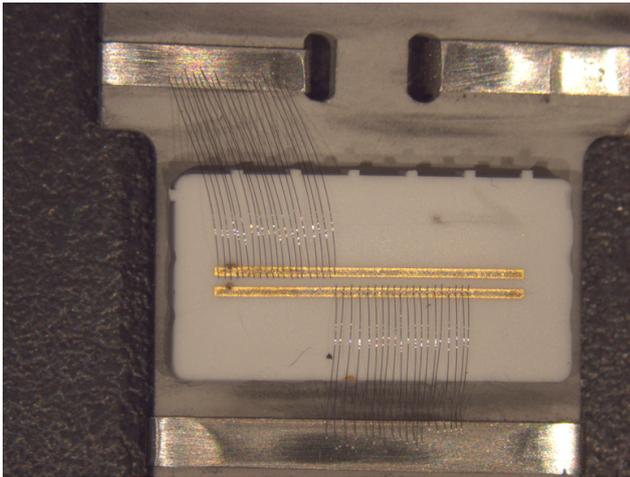


Figure 10. Closed LTCC device, mounted on a carrier. Twenty bonding wires of 25 μm in diameter hold the device in position and feed the signal in and out of the housing.

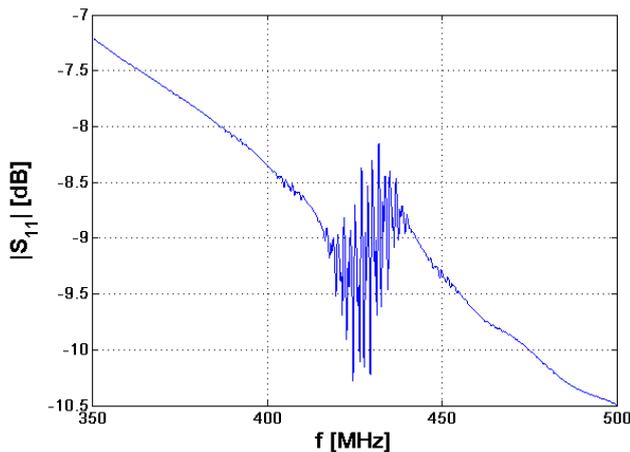


Figure 11. Device response to an interrogating sweep between 350 and 450 MHz. Scales are in decibels to enhance signal details. The blurred part at around 425 MHz is the device response – a superposition of three impulses with slightly different centre frequencies resulting in this interference pattern. Electrical crosstalk is distributed all over the signal resulting in this warped line.

RF interrogation was performed via reflective measurements of RF scattering parameters (S_{11}) from 370 to 470 MHz in 100 kHz steps using a vector network analyser (VNA). By doing this, the device is interrogated with a sine-shaped signal of a dedicated frequency and its response is compared to the reference. The differences between received interrogation signal and reference are calculated and stored. The next frequency (step) is tested likewise until all frequency steps have been interrogated. The achieved data matrix consists of frequency data points and corresponding, complex-valued device response data points, so-called scattering parameters, whose short form “S-parameters” is usu-

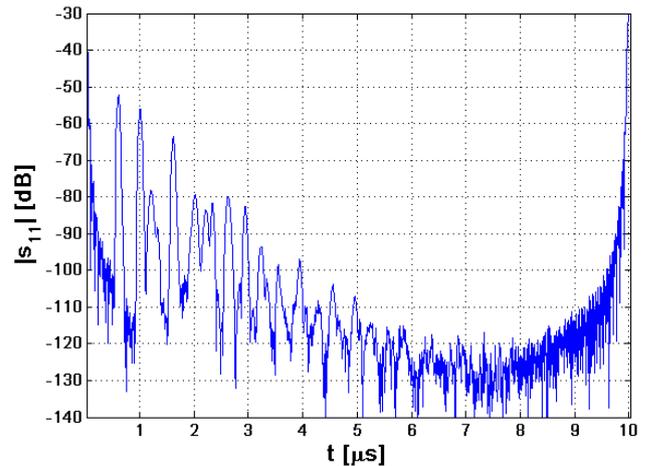


Figure 12. Impulse response of the measured signal from Fig. 11. Aside from the three impulses corresponding to the device design, there is a multitude of weaker peaks indicating echoes of the surface acoustic wave running back and forth on the crystal, leading to these artifacts.

ally used. Depending on the number of applied connectors of the VNA, called “ports”, the S-parameters are indexed (Hiebel, 2006; Zinke and Brunswig, 1999); in this case, port 1 is used as a sending and receiving port, and the short form of the only resulting S-parameter is written as “ S_{11} ”. These data are always recorded in the frequency domain. An exemplary plot is shown in Fig. 11.

From this signal, only qualitative assumptions can be made considering the functionality of the device. The main response energy is located at 425 MHz, as can be seen in Fig. 11. The blurred interference pattern is the result of the superposition of three impulses with different time delays and slightly different centre frequencies. This signal is processed as follows: a window is applied over its whole length to force the starting and ending points to the same value, preferably zero. This is needed to apply the inverse fast Fourier transform (IFFT) algorithm which can only be applied to periodic signals. The windowed signal is interpreted as one full period of the signal to be transformed, which allows the operation (Butz, 2003). The signal, in time domain, is shown in Fig. 12.

Figure 13 shows an enhanced area of Fig. 12 in which the main impulses of the device design are located.

Each one of these impulses is identified and analysed considering delay time, amplitude, and phase value at the maximum. This is possible as the measurement is complex valued and therefore includes amplitude and phase information of the signal. The impulses are multiplied each with a separate window. Thus, the signal becomes reduced to one single peak with surrounding zeroes which is transformed back to the frequency domain. This has to be done for each of the impulses separately. In Fig. 14, the result is shown after processing the data of one device. The algorithm is named time gating as a

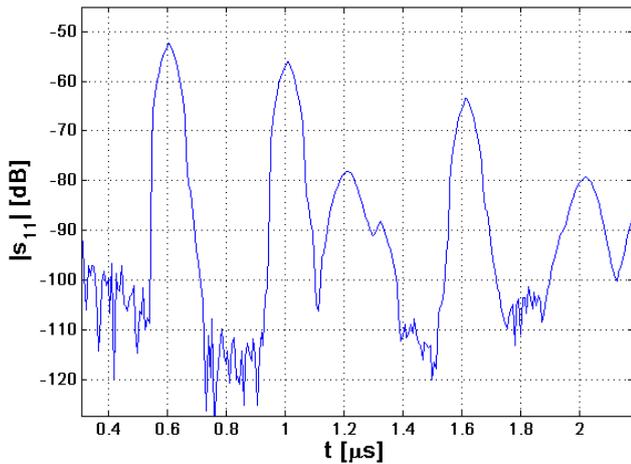


Figure 13. Detail view of Fig. 12. The main impulses show their dedicated maximum at around 0.6, 1, and 1.6 μs , respectively, and have the strongest amplitude in that area.

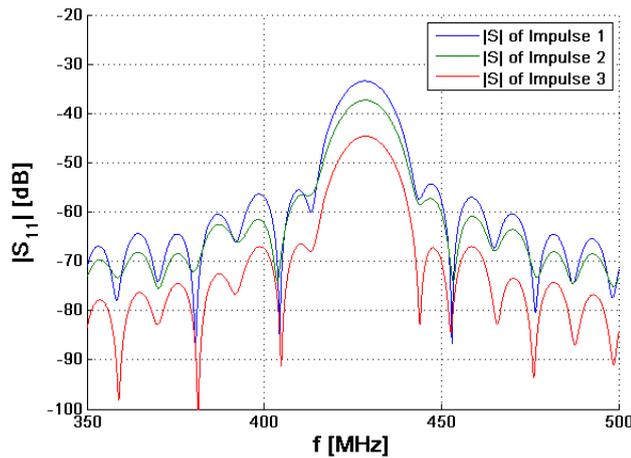


Figure 14. Transfer function of each impulse after time gating each single impulse and applying FFT.

window (gate) is applied in time domain. Again, the maximum is analysed regarding centre frequency, amplitude, and phase position.

Here, the transfer functions (TF) of the device for each single impulse are shown. The slight differences between these TFs result in an interference pattern, if superpositioned, as can be seen in Figs. 11 and 15.

All signal representations discussed previously are one-dimensional projections to the time or frequency axis, respectively. If the signal energy distribution is of interest – and sometimes, it is impossible to make out the signal from artifacts – a spectrogram can be used to analyse this energy distribution in the time–frequency plane (Boashash, 2015). Figure 16 shows the energy distribution of the tested device in this plane. The signal energy is concentrated in the main peaks (see Fig. 12) at around 430 MHz each. Sidelobes can

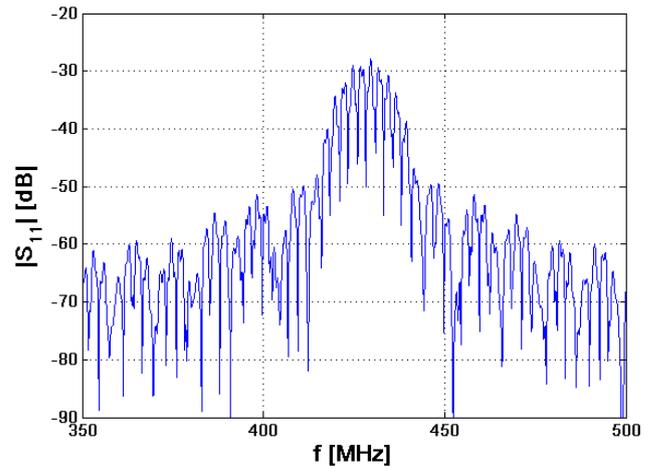


Figure 15. Interference pattern after superpositioning the TFs of all three main impulses. The difference to Fig. 11 is removed electrical crosstalk in this figure.

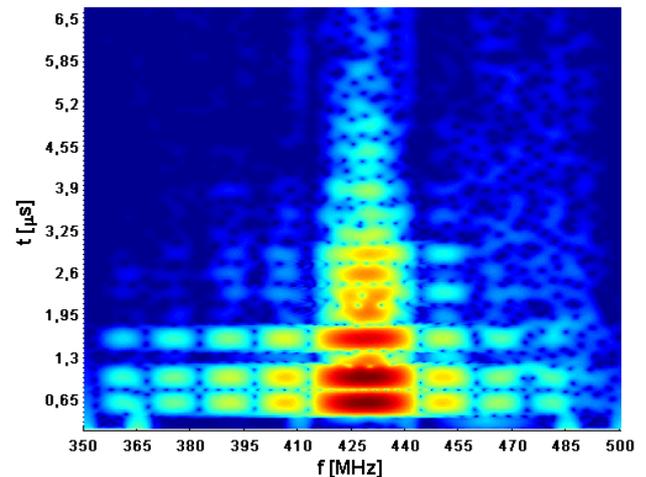


Figure 16. Spectrogram of the measured signal from Fig. 11.

be determined for each of the main peaks as separated circular areas in parallel to the frequency axis. Echoes from the chip edges and inter-IDT reflections can be seen at 430 MHz in between peaks 2 and 3 and after peak 3. As these artifacts show to have the same frequency as the SAW main signals, they are most likely SAW-based artifacts. Otherwise, the IDT would act like a frequency filter and suppress them.

After analysis of a measurement file, one single measurement point is done. Each of the dots in e.g. Fig. 17 is linked to one measurement. Thus, the whole measurement series is then condensed to line graphs showing the behaviour of an aspect of the device under the test circumstances, be it the centre frequency, the delay, or the corresponding amplitude and phase values.

It is expected that the analysed values change between temperature plateaus and stabilize during the time of 20 h in

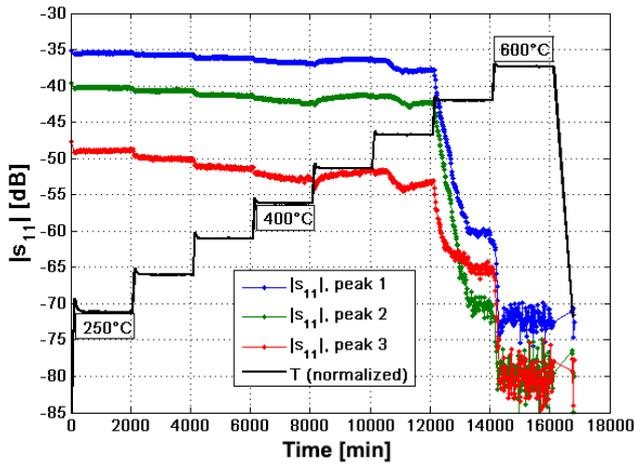


Figure 17. Amplitude values of the three impulses shown in Fig. 11 during the heat treatment. At 550 °C, amplitudes drop considerably and do not recover, indicating device failure.

which one such plateau is kept. Amplitude values might vary slightly by several decibels due to diffusion-driven resistivity changes of the platinum–aluminum thin film from which the electrodes are fabricated (Bardong, 2013; Bardong et al., 2010; Wall et al., 2015). Frequency, delay, and their corresponding phase values should stay constant on each individual temperature level and change due to the temperature coefficient of delay when a new temperature level has been set. As the phase value can be interpreted as the derivative of the observed main value (time or frequency), it is more sensitive to small changes and will therefore be preferably investigated (Smith, 2013).

Figure 17 shows the amplitude values of three impulses after evaluation of a complete measurement campaign. The normalized temperature levels are shown with the black line. The first level on the left indicates 250 °C, rising in 50 K steps to 600 °C on the right. Each vertical point triplet corresponds to a single measurement discussed earlier. The amplitude values do not change much due to temperature changes, but the temperature levels can be recognized as small step-like signal drops. At the second to last temperature level, the device shows amplitude degradation from –65 to –70 dB for all three impulses, which indicates a considerable degradation of the transducer structure leading to device failure by almost 21 dB (factor 128).

Whereas the amplitude holds the information of what happens to the metal layer during temperature treatment (Fig. 17), the phase values show shifts corresponding to temperature changes and indicate, with growing noise, device failure. Figure 18 shows the phase values of the first peak (blue line in Fig. 17) over time with a labelled, normalized temperature plot for comparison. The phase shifts can clearly be distinguished from one temperature level to the next. As the strong amplitude degradation occurs, the noise

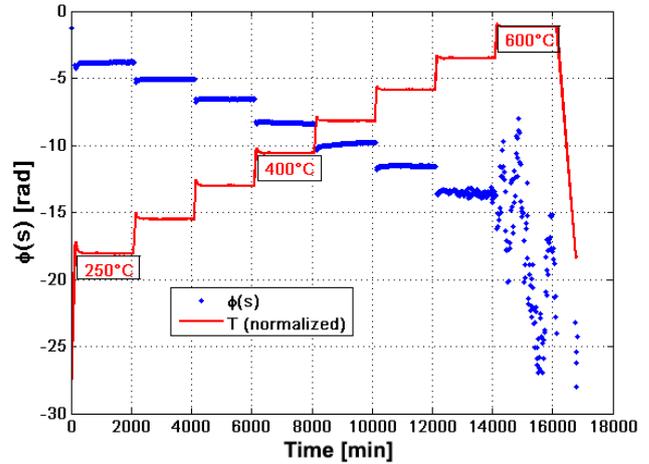


Figure 18. Phase response (dots) of a device’s first impulse (see Fig. 12 or 13 for a complete impulse response) during the temperature treatment (line).

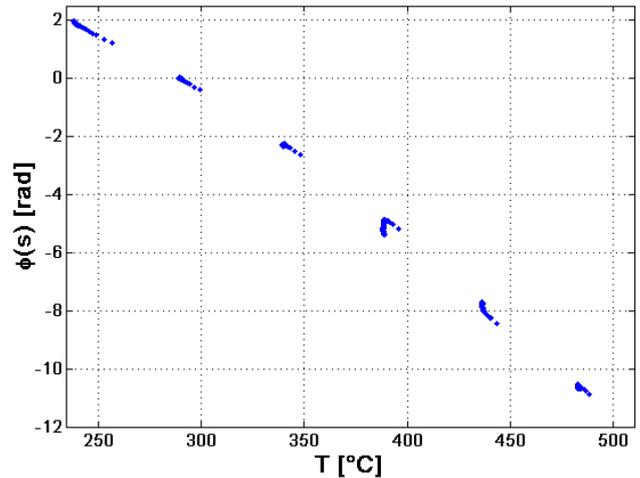


Figure 19. Phase response plotted over temperature.

of the phase readings rises slightly, but still allows it to match the temperature level of 550 °C with a device response. At 600 °C, device failure is indicated by the wide-spread phase values.

To test if the crystal itself behaves as estimated, the phase values of the first impulse maximum are plotted over the applied temperature. As expected, a slight parabolic behaviour of this crystal cut can be observed in this temperature regime (Hornsteiner, 1999; Naumenko and Solie, 2001; Malocha et al., 2002).

4 Results

During annealing, the devices showed good signals up to 500 °C (Figs. 17 and 18). Above this temperature, degradation occurred. This was not expected as non-housed de-

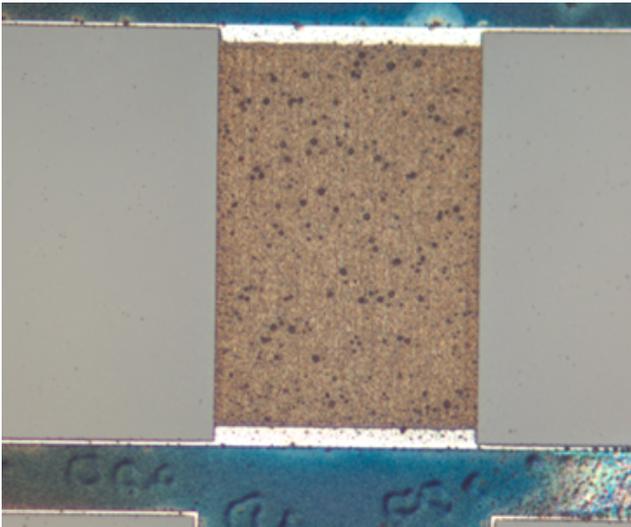


Figure 20. Detail of Fig. 8, centre structure, 200 times enhanced. Several dots on the finger structures indicate metal droplets leading to electrical shortcuts on the structure.

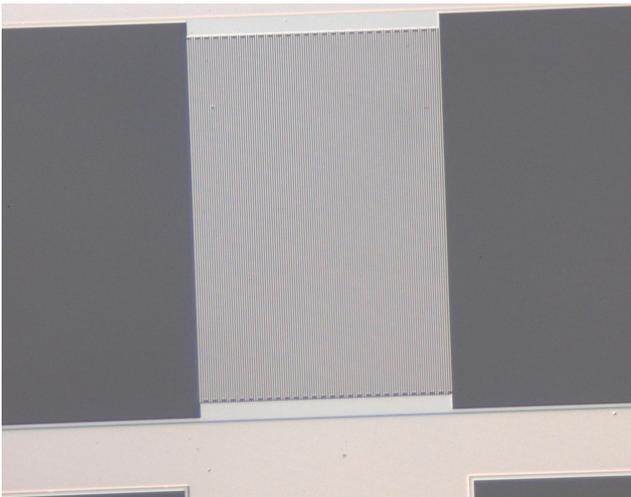


Figure 21. Structure before treatment, centre structure, 200 times enhanced. The finger area is clean of any droplet.

vices with similar design and equal Langasite and metallization material showed good stability at temperatures above 700 °C (Fig. 7) (Bardong, 2013). Optical analysis of the structures showed considerable recrystallization, dewetting and agglomeration of the metal layers as can be seen in Fig. 20. For comparison, an unaged device is shown in Fig. 21. The IDT area shows no dotted pattern.

Mass spectroscopy examination in the temperature range from room temperature up to 600 °C showed several mass counts matching with carbon oxides and carbon alone at the beginning of the treatment (Fig. 22). As this chemical compound can lead to a catalytic degradation of aluminum and its oxide, especially if platinum is present, which by itself is

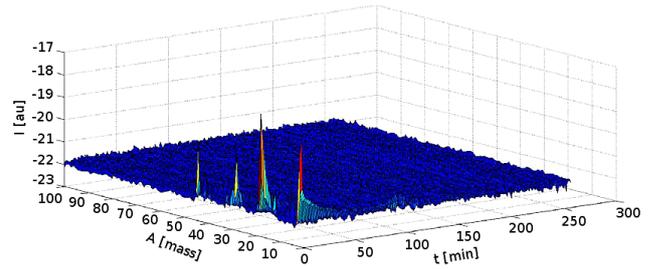


Figure 22. Effusion test graph of one device from room temperature up to 600 °C. At the very beginning of the examination, several mass counts occur, but during annealing, no additional counts are registered, indicating a volatile behaviour of the contaminants.

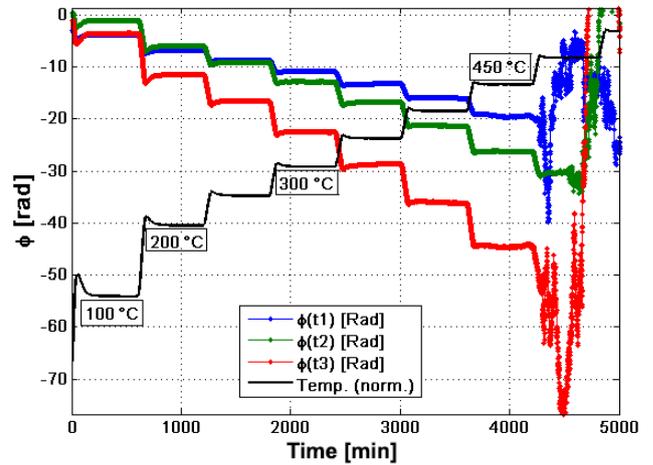


Figure 23. Phase values of a device from the second batch. Device failure above 450 °C has been reproduced.

a very good catalyst, a first assumption leads to reduce the contamination of the system with carbon-based compounds.

5 Further measurements and analysis

Based on these results and assumptions, a second batch of LTCC-housed Langasite devices was produced and measured.

To eliminate possible residual organic compounds inside the housing, the mounted devices were pre-annealed with open lids at 650 °C under oxygen for at least 2 h. The sealing of the lid was done afterwards at 550 °C after application of the glass seal paste under clean room conditions.

However, the previous results were reproduced: all devices failed at temperatures above 450 °C. In Fig. 23, the phase values of an exemplary device from this batch are shown. Again, agglomeration phenomena on the metal layer were observed.

Elementary analysis showed a considerable amount of Bi in the metal system. This explains the reduction of the metal system’s melting point as bismuth (Bi) is added to reduce ac-

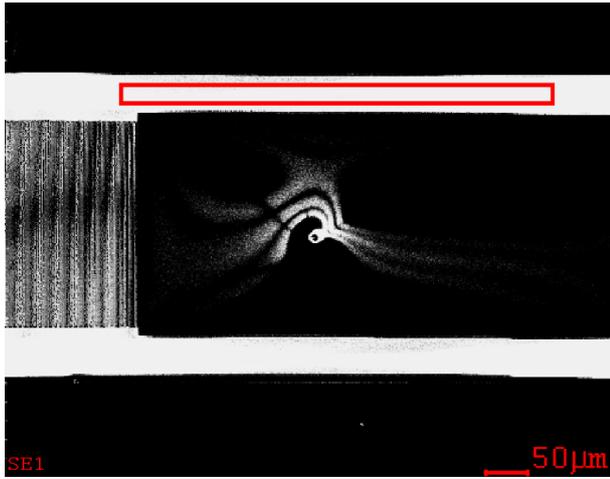


Figure 24. SEM photography of a new device. An area is marked for the elementary (FIB) scan. The IDT structure can be seen on the left between the two bright bus bars. The moiré-like pattern in the centre of this figure results from surface charges due to the SEM scan on this non-conductive, piezoelectric area.

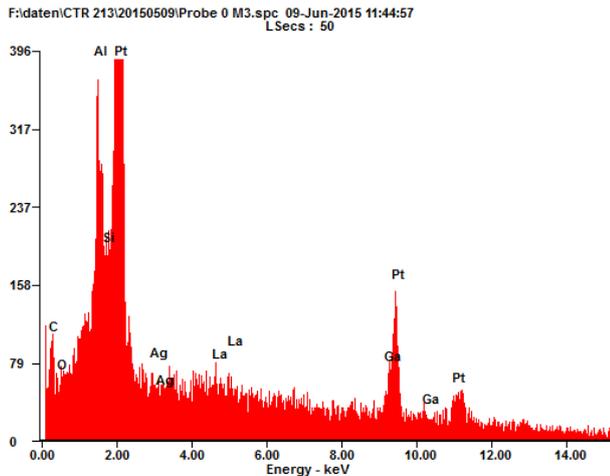


Figure 25. Distribution of elements along the area marked in red in Fig. 24. Mostly Pt and Al, the layer components, are detected and spurious signals of the crystal components like gallium (Ga), lanthanum (La), or silicon (Si).

tivation energies of soldering and sintering processes, mostly as a replacement of lead (Pb).

Figure 24 shows a SEM picture of a new chip. The structured metal layer shines bright white, whereas the Langasite shows some minor scattering patterns between the metallic bus bars in the centre of the figure. A FIB scan was performed inside the red marked area, the results are shown in Fig. 25. No bismuth was found.

Figures 26 and 27 show a device after heat treatment and the distribution of elements from the marked area, respectively.

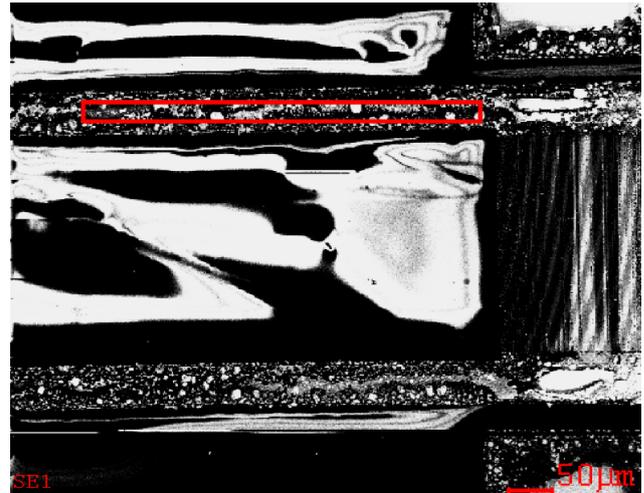


Figure 26. SEM photography of a device after heat treatment. The metallic bus bars show considerable increase in surface roughness. The area in the red box was subject to elementary analysis.

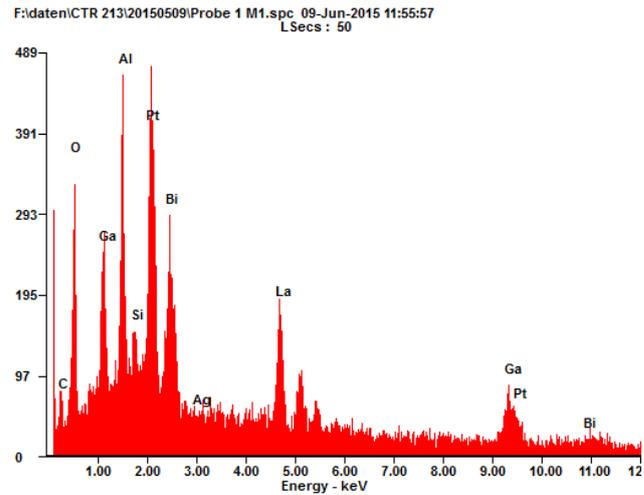


Figure 27. Distribution of elements of the marked area from Fig. 26. The contaminant Bi is detected.

Here, Bi is detected. This indicates that the Bi source is either the housing itself or an assembly component inside it after the seal is applied.

Further FIB scans of housing parts revealed the glass sealant as Bi source. Figure 28 shows the elementary distribution and the corresponding composition in weight and atomic percent.

6 Conclusions and outlook

The limiting factor of the devices considering the maximum temperature was not, as expected, an increase in conductivity of the LTCC leading to an electrical shorting of the signals. It was a contamination of the housing's atmosphere with

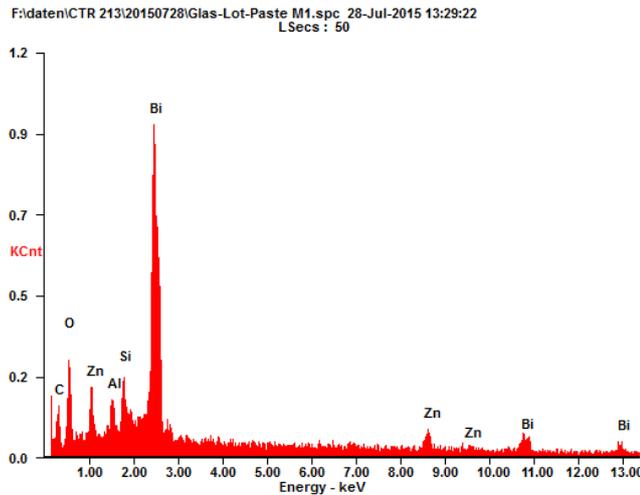


Figure 28. Elementary distribution of glass sealing paste. Bi shows the most exalted peak of all components.

evaporated Bi leading to agglomeration effects of the chip's metal layer and electrical shorting of the IDT fingers. As the sealing containing Bi as a sintering additive to lower the sintering temperature is heated to its glass temperature of about 550 °C, the material becomes more and more liquid, allowing the Bi to enter the gas phase inside the housing. Due to the high volatility of Bi, this element might be able to leave the compound already at lower temperatures. As the temperature profile is always completely executed, the device is treated with temperatures up to 650 °C, allowing the contaminant to leave its containing glass seal area.

This leads to the assumption that without this contaminant, the devices are operable above 450 °C.

Therefore, an alternative sealing strategy has to be tested. To avoid Bi and similar components that are likely to evaporate and contaminate the Pt–Al layer of the chips, metal sealants should be taken into account, e.g. silver–copper (Ag–Cu) based active solders.

The next steps will be tests of several active solders based on Ag and Cu and alternate sealing strategies like ceramic gluing without sintering additives like Bi and Pb. Taking this into account, the devices have potential to be used at temperatures of 500 °C and above.

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