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An ultra-low noise capacitance to voltage converter for sensor applications in 0.35 µm CMOS

Alexander Utz[1], Christian Walk[1], Norbert Haas[1], Tatjana Fedtschenko[1], Alexander Stanitzki[1], Mir Mokhtari[2], Michael Görtz[1], Michael Kraft[3], and Rainer Kokozinski[1,4]

[1]Fraunhofer Institute for Microelectronic Circuits and Systems (IMS), Finkenstr. 61, 47057 Duisburg, Germany
[2]Mir Enterprises Limited, 173c Goldhurst Terrace, Hampstead, London, NW6 3ES, UK
[3]Montefiore Institute, University of Liege, Rue de la Decouverte, 4000 Liege, Belgium
[4]Department of Electronic Components and Circuits, University of Duisburg-Essen, Bismarckstr. 81, 47057 Duisburg, Germany

Correspondence to: Alexander Utz (alexander.utz@ims.fraunhofer.de)

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Abstract. In this paper we present a readout circuit for capacitive micro-electro-mechanical system (MEMS) sensors such as accelerometers, gyroscopes or pressure sensors. A flexible interface allows connection of a wide range of types of sensing elements. The ASIC (application-specific integrated circuit) was designed with a focus on ultra-low noise operation and high analog measurement performance. Theoretical considerations on system noise are presented which lead to design requirements affecting the reachable overall measurement performance. Special emphasis is put on the design of the fully differential operational amplifiers, as these have the dominant influence on the achievable overall performance. The measured input referred noise is below 50 zF/$\sqrt{\text{Hz}}$ within a bandwidth of 10 Hz to 10 kHz. Four adjustable gain settings allow the adaption to measurement ranges from ±750 fF to ±3 pF. This ensures compatibility with a wide range of sensor applications. The full input signal bandwidth ranges from 0 Hz to more than 50 kHz. A high-precision accelerometer system was built from the described ASIC and a high-sensitivity, low-noise sensor MEMS. The design of the MEMS is outlined and the overall system performance, which yields a combined noise floor of 200 ng/$\sqrt{\text{Hz}}$, is demonstrated. Finally, we show an application using the ASIC together with a CMOS integrated capacitive pressure sensor, which yields a measurement signal-to-noise ratio (SNR) of more than 100 dB.

1 Introduction

Capacitive sensors are widely used for the accurate measurement of physical quantities such as pressure, acceleration or orientation. Such sensors have low temperature dependence, low power consumption and low noise compared to other technologies. In recent years, there have been quite a number of development activities on micro-electro-mechanical system (MEMS) based capacitive accelerometers and gyroscopes (Yazdi and Najafi, 1997; Zhang et al., 1999; Bernstein et al., 1999). Such MEMS sensors are fabricated either in surface or bulk micromachining technology. These technologies can be compatible with existing VLSI production processes like CMOS or SiGe-BiCMOS and allow seamless combination with the readout circuit or even monolithic integration (Ruan et al., 2012; Wang et al., 2011; Rudolf et al., 2014).

In contrast to sensors built from discrete mechanical elements, MEMS based solutions have suffered, and still suffer, from a significantly increased noise level and thus reduced measurement performance. A mechanical noise source within the MEMS element itself is the Brownian noise induced by the thermal motion of the air atoms inside the MEMS package. There are multiple methods for reducing the MEMS noise and increasing the measurement dynamic range (DR), including vacuum sealing of the sensing structure or electrostatic feedback (Chen et al., 2014). Applications such as seismic measurement or highly sensitive vibration detection, e.g., crucial in earthquake early detection or

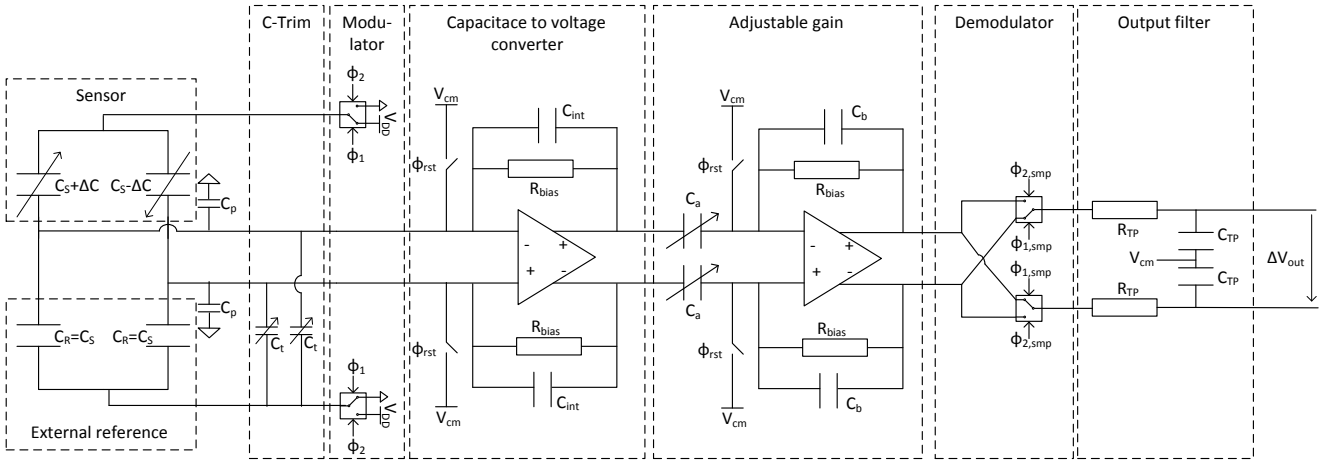


Figure 1. Block diagram of the presented circuit architecture.

vibration monitoring of buildings, require noise levels significantly below 1 µg/$\sqrt{\text{Hz}}$. Current sensor MEMS reach noise levels of as low as 100 ng/$\sqrt{\text{Hz}}$, which allow their use in such applications.

The readout IC's (ROIC) electrical noise adds to the MEMS's mechanical noise. For highly optimized MEMS sensors with high sensitivity and low mechanical noise contribution, the ROIC becomes dominant. Therefore, the reduction of input referred electrical noise becomes the most important parameter in the ROIC design for such MEMS sensors. The design of a low-noise ROIC is detailed in Sects. 2 and 3 of this paper.

Similar sensor systems were presented in Kajita et al. (2001), Amini and Ayazi (2004), Georgakopoulou et al. (2016) and Jiang et al. (2012), which focus on the direct digitization of the measurement signal. The major drawback of such solutions, together with higher power consumption, is the extra amount of electrical and quantization noise from the ADC, which adds to the analog frontend's noise and thus reduces the system's DR. Therefore, the focus of this work was to create an ASIC (application-specific integrated circuit) with an ultra-low noise analog differential interface. Digitizing and post-processing is then done by external system components which can be chosen to meet the requirements of the specific application.

Other ROICs have been presented previously, focusing on the analog frontend or the monolithic integration of sensing element and ROIC (Yazdi et al., 2004; Wu et al., 2004; Tavakoli and Sarpeshkar, 2003). The noise level of the ASIC presented in this work was significantly reduced compared to previous work by putting a special focus on the operational amplifiers during the design phase.

To demonstrate the versatility and performance of the developed ROIC, two system implementations, using capacitive sensors for different physical quantities, are demonstrated.

1. MEMS based accelerometer from Mir Enterprises Ltd.: the measurement performance of a complete high-sensitivity, low-noise acceleration measurement system containing the ROIC from Fraunhofer IMS and the sensing element from Mir Enterprises will be demonstrated in Sect. 6.

2. Pressure sensor from Fraunhofer IMS: the design of a CMOS integrated pressure sensor in 1.2 µm CMOS, extended by dedicated process steps to implement the pressure sensitive elements, will be introduced and its performance in combination with the developed ASIC will be described in Sect. 7.

2 Architecture of the C/V conversion stage

Figure 1 shows a block diagram of the analog frontend of the developed readout circuit. The sensing element is connected via a fully differential four-wire interface. A capacitive bridge configuration has to be formed by the sensor and additional external or internal components. To allow direct connection of sensors with low nominal capacitances and to allow the trimming of imbalances in both branches of the capacitive bridge (e.g., due to parasitics and wiring imperfections), two switchable banks of trim capacitances are implemented on-chip. The resolution of this capacitance banks is 8 bit with an LSB step size of 20 fF. That allows connection of a maximum capacitance of 2.56 pF internally. For sensors with higher nominal capacitance, additional external reference capacitors have to be provided.

Two of the ASIC external connections are used as outputs and provide the stimulation voltage for the sensing bridge. The other two are the actual sensing inputs internally held at 2.5 V, which is the common mode voltage of the fully differential charge amplifier.

The core of the readout circuit forms a two-stage, fully differential, chopper-stabilized amplifier. The first stage per-

forms the actual capacitance to voltage (C/V) conversion. It is an AC-coupled, fully differential, two-stage operational transconductance amplifier (OTA) with a class AB output stage. The feedback capacitor C_{int}, together with the input differential capacitance ΔC of the sensing element, determines the overall closed-loop voltage gain of the amplifier stage. The excitation voltage is a square wave with a constant amplitude of V_{DD} (i.e., 5 V). Thus, the output voltage of the first stage varies with varying differential capacitance of the MEMS sensing element. The governing capacitance to voltage conversion equation is given by

$$V_{\text{c2v}} = 2\frac{\Delta C_{\text{s}} \cdot (V_{\text{DD}} - V_{\text{cm}})}{C_{\text{int}}}. \tag{1}$$

The second stage is implemented to allow the selection of multiple full scale measurement ranges (FSRs). The total amplification is adjustable in four steps between a factor of 1 and 4. This corresponds to a measurement range for ΔC between ± 0.75 and ± 3 pF. The gain of the second stage is given by

$$G_2 = \frac{C_a}{C_b}. \tag{2}$$

With post-amplification of the output voltage by the second amplifier stage, the total output voltage of the analog front-end becomes

$$\Delta V_{\text{out}} = G_2 \cdot V_{\text{c2v}} \tag{3}$$

and the overall measurement sensitivity in units of V F^{-1} is

$$S_{\text{c2v}} = \frac{\Delta V_{\text{out}}}{\Delta C_{\text{s}}} = 2G_2\frac{V_{\text{DD}} - V_{\text{cm}}}{C_{\text{int}}}. \tag{4}$$

The amplifier stages are followed by the demodulator, which transforms the carrier based signal generated by the square wave excitation voltage back into the baseband and vice versa shifts any accumulated low-frequency noise from the baseband to the carrier frequency.

The final component of the analog front-end is an output low-pass filter that band-limits the output signal and thus eliminates the high-frequency noise components.

The proposed sensor interface allows the connection of single-ended or fully differential capacitive sensors in full or half bridge configuration either with or without external reference capacitors, depending on the type and characteristics of the sensing element used.

3 Low noise design considerations

The main design goal for the presented ROIC was measurement accuracy. Besides the uncertainty of the connected sensing element, self-generated noise of the electrical components in the ROIC is the limiting factor. The dominant noise sources in electronic systems such as the one described here are thermal and flicker (or $1/f$) noise. For a high gain of the first amplifier stage, the overall noise is determined by the noise components introduced by the transistors of its input differential pair and the feedback network (Leach, 1995). There are three distinct noise sources in the circuit architecture presented in Fig. 1:

1. noise of the operational amplifiers p_A,
2. noise of the feedback network p_B and
3. noise generated by the output filter p_C.

For low frequencies, the flicker noise components are dominant over the thermal noise ones (Ana, n.d.). The amount and shape of flicker noise introduced are technology and operating point dependent. To allow accurate low-frequency measurements, it is crucial to effectively reduce this influence by adequate circuit design techniques.

Techniques for flicker noise reduction include autozeroing, correlated double sampling and chopper stabilization (Enz and Temes 1996). As the first two come along with sampling of the measurement signal, an effect known as noise folding leads to increased white noise (and thus increased total system noise) in the baseband. This disadvantage is avoided in a chopper stabilized system because the process of modulation and demodulation does not increase baseband noise (Yin et al., 2006; Enz et al., 1987). For a chopper stabilized amplifier, the total noise power can be calculated as (Yin et al., 2006; Kevin et al., 2010)

$$p_A = \gamma_{\text{n}} \cdot \frac{16}{3}\frac{k_{\text{B}}T}{g_{m0}} \cdot \left(1 + \frac{17 f_k}{2\pi^2 f_{\text{chop}}}\right) \cdot \eta, \tag{5}$$

where γ_{n} is the noise excess factor, k_{B} the Boltzmann constant, T the absolute temperature, g_{m0} the transconductance of the input transistors, f_k the flicker noise corner frequency and f_{chop} the chopping frequency. η is a complexity factor which takes into account all noise sources additional to the input differential pair. It will be derived for the chosen amplifier architecture in Sect. "The operational amplifiers". γ_{n} is assumed to be on the order of 1.5 for the specific input stage transistors operating in moderate inversion (Goo et al., 2001).

The second source of noise that has to be taken into account is the noise introduced by the feedback network, consisting of a resistor and a capacitance to set the desired loop gain. The thermal noise introduced by the feedback can be calculated as (Kevin et al., 2010)

$$p_B = \frac{8k_B T R_{\text{bias}}}{1 + 4\pi^2 R_{\text{bias}}^2 C_{\text{int}}^2 f_{\text{chop}}^2}. \tag{6}$$

The feedback resistor R_{bias} forms a leakage path to stabilize the input common mode voltage against drift and is on the order of several $M\Omega$. It is implemented as a diode chain operating in the sub-threshold region. Therefore, noise from the feedback network becomes small compared to amplifier noise and hence negligible.

The same equations apply for the second amplifier stage. The amplifier input noise is amplified with its noise gain; the feedback network noise directly transfers to the output of each stage. Thus, the output noise power density for each stage is

$$p_{O1/2} = p_A\left(1 + G_{1/2}\right)^2 + p_B, \tag{7}$$

where G_1, the voltage gain of the first stage, is given by

$$G_1 = \frac{2C_\mathrm{s} + C_\mathrm{p}}{C_\mathrm{int}}. \tag{8}$$

G_2, the voltage gain of the second stage, has already been defined in Eq. (2). The last source of noise is the output low-pass filter. For an implementation as a passive RC filter, its noise density is determined by the resistor's thermal noise:

$$p_C = 4k_B T R_\mathrm{TP}. \tag{9}$$

The total output noise power density of the two-stage C/V converters is then given by

$$p_O = p_{O1} G_2^2 + p_{O2} + p_C. \tag{10}$$

The dominant source in this equation is the amplifier noise p_A of the first stage. If the gains in the amplifier stages become small, however, the noise of the output filter p_C becomes significant and must be considered.

The input referred noise with respect to the input of the first OP, which is typically used as the loop gain independent performance figure for an amplifier and can be calculated from the total output noise power and the voltage gain as follows:

$$p_i = \frac{p_O}{(1 + G_1)^2 \cdot G_2^2}. \tag{11}$$

The equation above gives the input referred noise power in units of $\mathrm{V^2\,Hz^{-1}}$. The actual quantity to be measured is a change in the sensor capacitance ΔC_s. Therefore, a more meaningful figure for the overall measurement accuracy is the input referred noise amplitude density in means of capacitance fluctuation (given in $\mathrm{F}/\sqrt{\mathrm{Hz}}$):

$$n_i = \frac{\sqrt{p_O}}{S_\mathrm{c2v}}. \tag{12}$$

This figure is a function of the sensing element's nominal capacitance and the parasitic capacitance seen at the ROIC's inputs. That means sensing elements with low nominal capacitance are advantageous for the overall noise performance. System level optimization towards low C_p is also crucial. The objective of the presented design was to reach a noise level lower than $50\,\mathrm{zF}/\sqrt{\mathrm{Hz}}$ for the reasons stated in Sect. 1. The total theoretical input referred noise of a sensor system can then be calculated as

$$n_\mathrm{Sens} = \sqrt{\left(\frac{n_i}{S_\mathrm{s}}\right)^2 + n_\mathrm{s}^2}, \tag{13}$$

Table 1. OTA performance characteristics.

Parameter	Stage 1	Stage 2
Input stage	PMOS	NMOS
W/L in $\mu\mathrm{m}\,\mu\mathrm{m}^{-1}$	23 296/0.36	192/0.36
DC gain	90 dB	80 dB
Bandwidth	200 MHz	200 MHz
Slew rate	$3\,\mathrm{V}\,\mu\mathrm{s}^{-1}$	$3\,\mathrm{V}\,\mu\mathrm{s}^{-1}$
Current consumption	50 mA	4 mA
Max. cap. load	215 pF	15 pF
Input stage g_m	$130\,\mathrm{mA\,V^{-1}}$	$16\,\mathrm{mA\,V^{-1}}$

where S_s is the sensitivity of the sensing element (e.g., in $\mathrm{F\,g^{-1}}$ for an accelerometer MEMS) and n_s its mechanical noise contribution.

With maximum gain in the first amplifier stage of the ROIC and only minimal gain in the second stage, the overall electrical output noise is dominated by the noise of the first stage (Leach, 1995). The limiting factor is the minimum size of the integration capacitor C_int, for which process variations and device matching have to be considered. In this implementation a capacitor value of 100 fF was chosen.

From Eq. (5) it becomes obvious that the main parameters for noise reduction are the chopping frequency f_chop and the transconductance g_{m0} of the input stage.

The flicker noise corner frequency f_k depends on the actual transistor area and technology dependent parameters. For the transistor sizing shown in Table 1, Stage 1, in combination with the 0.35 µm CMOS technology used in this work, it is about 25 kHz. The chopping frequency for the C/V conversion stage has to be chosen so that

1. the second term in the parentheses of Eq. (5) becomes much smaller than 1 and
2. the resulting demands on the OP-Amp design towards slew rate and bandwidth are still realistic.

For the above two reasons, a chopping frequency of 833 kHz was chosen. Figure 2 shows the implemented clocking scheme for the chopper amplifier. To give the output sufficient time to settle, the sampling phase for the demodulator has a reduced duty cycle compared with the modulating signal.

After demodulation, the flicker noise power is shifted from the baseband to the modulation frequency at 833 kHz. To filter out these components, the final output filter band-limits the output signal. Although an active filter topology has advantages with respect to filter characteristics and noise reduction, it would also introduce additional flicker noise which would not be reduced by the chopper architecture. Therefore, the filter was implemented as a purely passive RC filter with a corner frequency of 80 kHz ($R = 100\,\mathrm{k\Omega}$, $C = 20\,\mathrm{pF}$). This low pass together with parasitic resistors and capacitances from switches, I/O pads and interconnects limits the overall

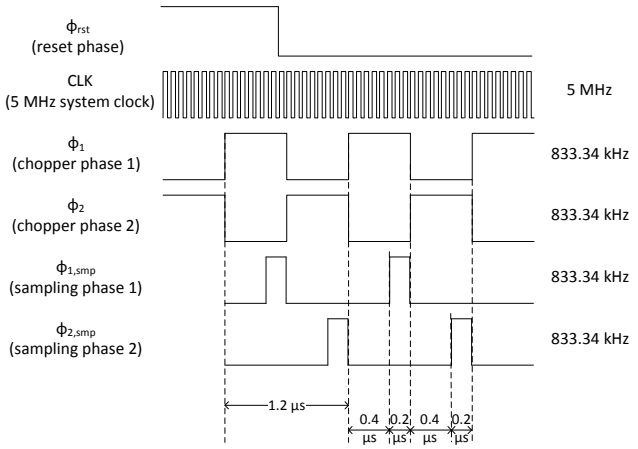


Figure 2. Clocking scheme for chopper and demodulator.

signal bandwidth. The resulting −3 dB bandwidth of the system is 51 kHz.

The contribution of flicker noise to the total output noise is thus reduced to a negligible amount. The implemented chopper architecture and selected frequencies come along with requirements on the operational amplifiers, which will be described in detail in the next section.

The operational amplifiers

The main performance criterion for the operational amplifiers in this application is the gain bandwidth product (GBW). The bandwidth dictates the maximum chopper frequency that can be used to separate the input signal from $1/f$ noise, while maximum gain is desirable to limit the number of required gain stages contributing to white noise (see above). In contrast, GBW can be traded against chip area, power consumption and input and output voltage range. The switching frequency was selected to 833 kHz.

A fully differential two-stage folded cascode architecture was selected with a push–pull output stage operating in class AB mode. The simplified circuit is shown in Fig. 3. The folded cascode input stage allows larger V_{DS} for the differential pair at a fixed 5 V supply voltage and the push–pull output stage isolates the output from the capacitive load, which varies with the selected system gain and depends on the nominal sensor capacitance.

The gain in the first stage was maximized by choosing a large tail current of 10 mA and optimizing g_m/I_D efficiency (the transistor's transconductance per unit drain current) by operating the input stage in moderate inversion with an overdrive voltage of around 10 times the thermal voltage V_T. An upper bound to the size of the input stage is set by the required switching speed and hence the requirement on the transit frequency f_T and the related pole at C_{par}/g_m, where C_{par} is mainly determined by the drain diffusion area of the differential pair transistors. Minimum gate length was hence chosen and folding applied during layout. The upper limit for the tail current was derived from the $V_{DS,sat}$ required to operate the tail current source, the cascade, the differential pair and the NMOS current source in saturation region at a minimum supply voltage of 4.5 V and a junction temperature of 85 °C. To increase the g_m per area ratio, thin gate-oxide transistors were used for the differential pair. Special care was taken to ensure V_{DS} exceeds neither the breakdown and punch-through limits of the thin gate-oxide device nor its long-term degradation limits. A PMOS input stage was selected because of its lower $1/f$ noise corner frequency in the selected technology, compensating for the lower g_m per area.

A continuous-time common mode feedback (CT-CMFB) was used to control the common mode output level of the amplifier. The main amplifier is shown in Fig. 3. The bias current and area ratios in the current mirror loop formed by M12, M13, M16 and M2m set the bias point for the PMOS of the push–pull output stage (Hogervorst et al., 1994). The bias point of the NMOS output transistor is likewise set by the loop formed by M15, M14, M17 and M3m. The bias currents depicted as current sources are on-chip generated references. In the balanced state, the bias points are selected for an output voltage of approx. $V_{DD}/2$. Mismatch in the translinear loop can shift the operating points of the NMOS and PMOS output transistors independently, especially in cross-corner situations. This mainly results in an output common mode level variation, compensated for by the CMFB. The common mode voltage is controlled by tuning the current at the source of M16 using the outputs cmfb_p/m of the CMFB regulator.

The CMFB regulator is shown in Fig. 4. The overall control loop includes two non-inverting gain stages in the CMFB regulator and the inverting main amplifier output stage. This allows overall compensation feedback from the main amplifier output to the first stage of the CMFB regulator, which makes frequency compensation of the CMFB independent of the compensation of the main amplifier.

Due to stability issues a cascode for the PMOS current sources at cmfb_p/m was removed, which also lowers the gain in the signal path of the amplifier. For future work it is planned to re-insert the cascode to improve overall performance.

Significant contributions to the overall amplifier noise, additional to the input differential pair, are induced by the current source transistor pairs M5–M7 in the main amplifier and M8–M9 and M14–M15 in the CMFB amplifier. The noise current of these transistors propagates directly to the amplifier output. Thus, the complexity factor η introduced in Eq. (5) can be calculated as

$$\eta = 1 + \frac{g_{m5}}{g_{m0}} + \frac{g_{m8,\mathrm{CMFB}}}{g_{m0}} + \frac{g_{m14,\mathrm{CMFB}}}{g_{m0}} \tag{14}$$

and is 1.38 for the first stage amplifier. The gain of the second stage can be selected, via a switched capacitive feedback network, to accommodate the desired measurement range and

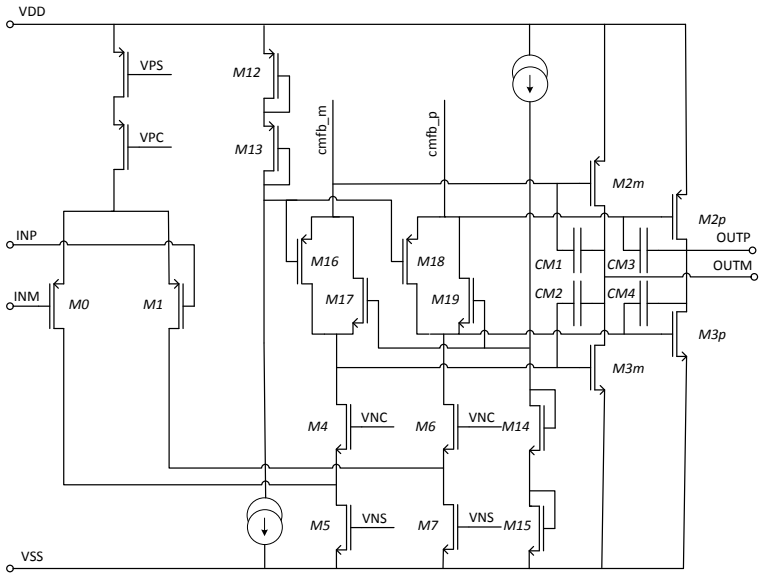


Figure 3. Architecture of the fully differential class AB OTA.

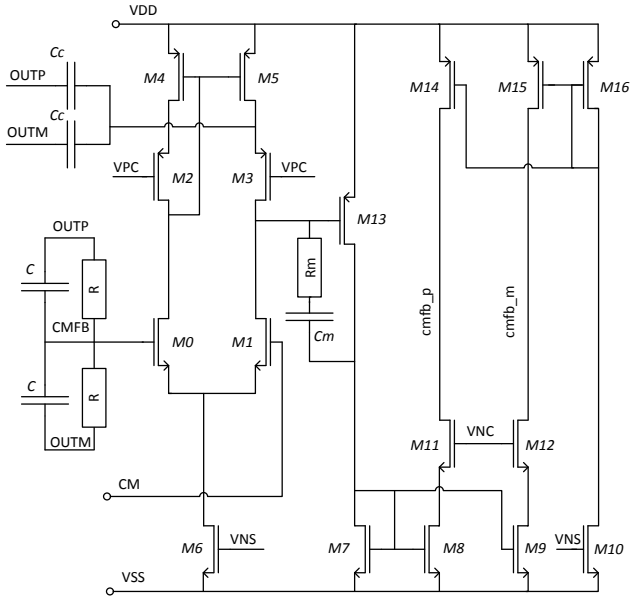


Figure 4. Architecture of the common mode feedback.

output voltage swing. The minimum selectable gain is two. Thus, the load for the first amplifier coming from the second amplifier varies between 5 and 20 pF. The additional load resulting from the feedback capacitor C_{int} (see Fig. 1) is 2 pF. In order to maximize the OTA's bandwidth per power, the frequency compensation of the second stage was designed for stability at a minimum gain of two, i.e., deliberately not unit-gain stable. This results in a bandwidth increase of approximately half a decade. Compared to the stage one amplifier, several requirements for the second stage are relaxed.

1. The required DC gain is lowered because of the reduced closed-loop gain in the second stage.

2. The $1/f$ noise contribution is less critical since it is not amplified by a succeeding stage. An NMOS input stage was hence used.

3. The capacitive output load is independent of the sensor capacitance and can be made small. The current consumption and area could thereby be reduced at the cost of a lower driving capability.

4 Overall ASIC architecture

Figure 5 shows the overall architecture of the developed ASIC. The total chip area is 3.5 mm × 3.5 mm in a 0.35 µm process. The core C/V conversion unit was described in detail above. The output of the low-pass filter is directly connected to pads and also fed into an output buffer which is realized as an instrumentation amplifier, which has a current consumption of about 1.5 mA. This buffered output allows resistive loads of 100 kΩ and more. The drawback is the additional flicker noise introduced by the OPs in the instrumentation amplifier, so the noise level of the buffered output is increased compared to the unbuffered output. For very high noise requirements, the unbuffered output shows a significantly improved noise performance. An external buffer with very low noise characteristics (e.g., with JFET input stage) can be used to drive resistive loads in combination with very high accuracy requirements.

A bandgap reference provides an absolute voltage reference for supply regulation and brown-out detection. An internal LDO generates the 3.3 V supply for these blocks from

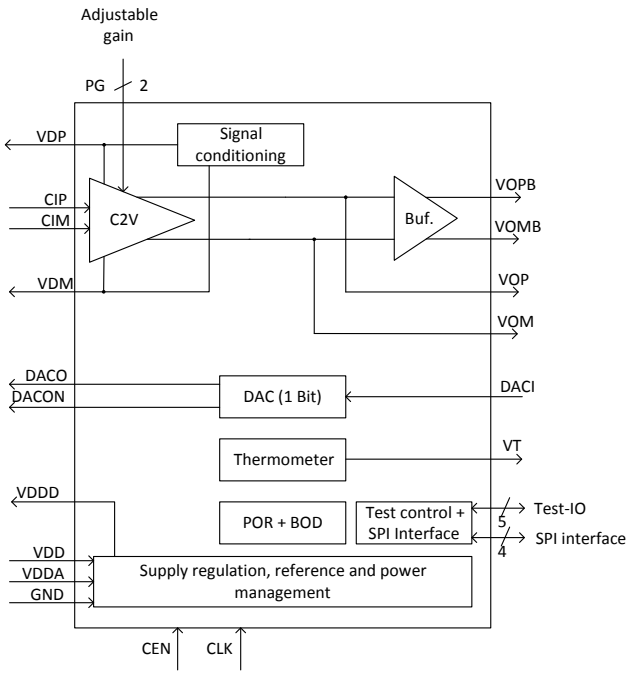


Figure 5. Block level schematic of the complete readout ASIC.

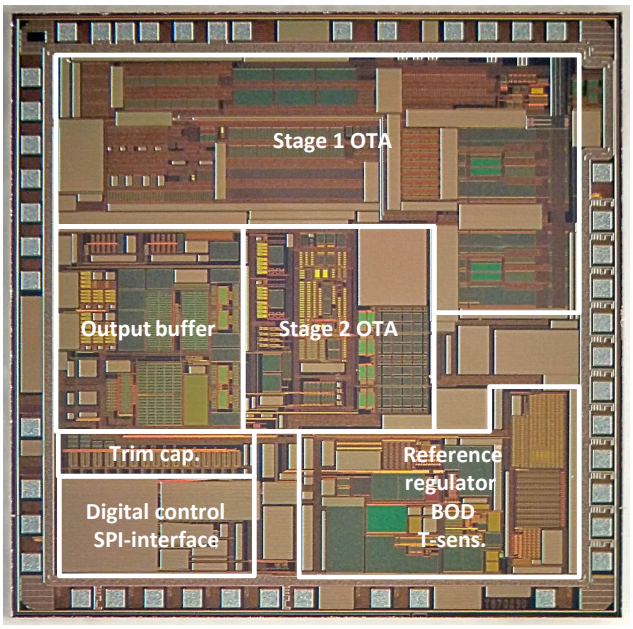


Figure 6. Photograph of the chip.

the externally supplied 5 V V_{DD}. The integrated brown-out detection puts the chip into reset state if the supply voltage falls below a critical limit.

The signal conditioning for modulation and demodulation signals (clocking scheme generation and non-overlap circuitry) together with the digital test interface and serial peripheral interface (SPI) were implemented using digital standard cells in 3.3 V logic. The internal trim capacitors can be configured via the SPI interface.

It is also possible to equip the analog ROIC with an internal ADC to provide 13 bit digitized measurement data on a parallel digital interface. As the control logic of the ADC runs at relatively high frequencies and interference with the analog frontend is expected, this ADC is not present in this version of the chip, where maximum analog accuracy is crucial.

Finally, a temperature sensor with a sensitivity of 15 mV/K and an accuracy of ±1 K within a temperature range from −40 to 65 °C allows monitoring of the chip temperature. The temperature value is output as a single-ended voltage and helps to calibrate temperature effects at system level. The knowledge of the actual temperature together with a known temperature behavior of the sensor systems enables the correction of measurement results on system level, e.g., by post-processing the measurement values in a microprocessor.

Figure 6 shows a photograph of the ASIC with the different building blocks labeled. The sensor interface allows the connection of different types and configuration of capacitive sensors. Figure 7 illustrates the possible interconnections. Sensors such as accelerometers with three electrodes can be connected using reference capacitors for the lower half of the measurement bridge (Fig. 7a). For fully differential sensors (e.g., presented in Zhang et al., 1999), as well as for sensors with a nominal capacitance less than or equal to 2.5 pF, these reference capacitors can be omitted (Fig. 7b and c). Single-ended sensors with only two electrodes can also be connected as illustrated in Fig. 7d.

5 Measurement results

Measurements on the developed IC were performed inside a climatic chamber to provide well-controlled temperature conditions and also shield against environmental interference. The 5 V supply voltage was generated by a laboratory voltage source of type Agilent E3649A and the 5 MHz system frequency by an Agilent 33220A Waveform Generator. Measurements of the output voltages were done with Keithley™ 2000 Multimeters and an Agilent 35670A Signal Analyzer was utilized to do the noise measurement. Figure 8 shows the output voltage of the readout IC at its unbuffered output as a function of input differential capacitance. The capacitance difference was applied using the internal trim capacitors. It can be seen that the transfer curve has linear dependency in a wide voltage range from approximately −4 to +4 V. The resulting conversion factors for the different gain settings are summarized in Table 2. There is an offset in the measured capacitance of 640 fF which results in a horizontal shift of the measured transfer curve (corresponding to about 22 % of the measurement FSR for the lowest and about 87 % for the highest gain setting). The reasons for this offset are differences in the parasitic capacitances between the mea-

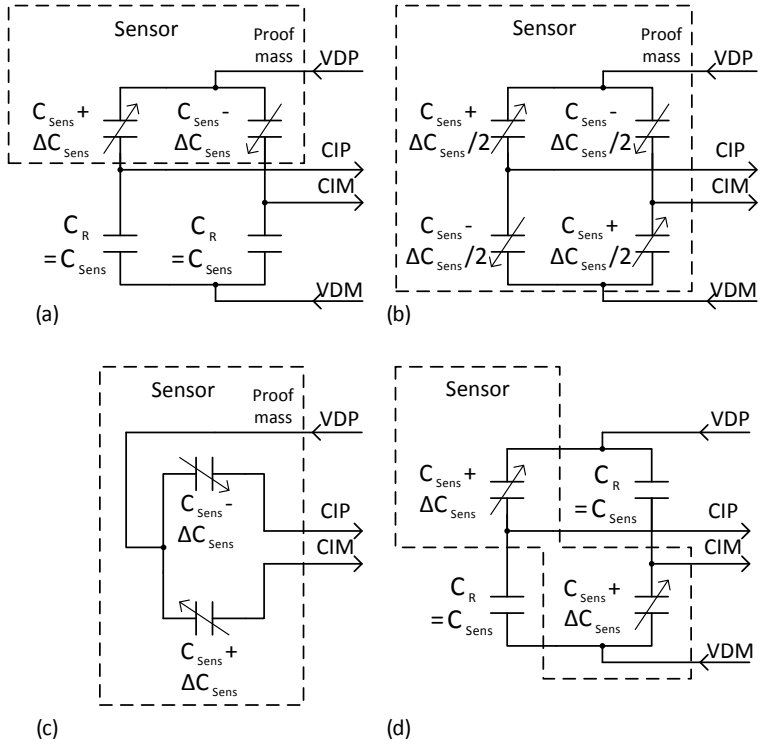


Figure 7. Connection schemes for different types of sensing elements: **(a)** differential sensing element using reference capacitors; **(b)** fully differential sensing element without external devices; **(c)** differential sensing element with low nominal capacitance and **(d)** single-ended sensing element.

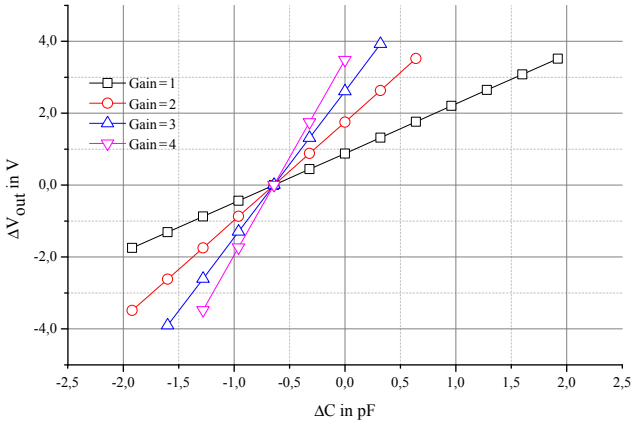


Figure 8. Measured capacitance to voltage transfer curves for the four gain settings.

Table 2. Performance parameters of the developed ASIC.

Gain setting	Sensitivity ($V\,pF^{-1}$)	Output noise density ($nV/\sqrt{Hz}$)	Input referred noise density ($zF/\sqrt{Hz}$)	Dynamic range (dB)
1	1.37	135.33	98.78	130
2	2.74	163.61	59.71	128
3	4.08	204.69	50.17	126
4	5.44	254.32	46.75	124

surement inputs CIM/CIP and the excitation voltage outputs VDM/VDP, resulting from mismatches in the system PCB (printed circuit board) and assembly as well as process mismatch during the ASIC fabrication. The measured offset is approximately constant for measurement on multiple devices from the same wafer on the same test PCB.

The noise amplitude spectral density was measured with fixed capacitances at the input of the circuit. The nominal sensor capacitance (between CIM/CIP and VDM/VDP) was measured as 5 pF, the parasitic capacitance between CIM/CIP and system GND as 13 pF. Figure 9 shows the measured input referred noise density. The peak observed at 50 Hz and its odd harmonics come from power supply interference and reflect the frequency of the 230 V supply net. These disturbances can be avoided using a battery powered supply. Table 2 summarizes the resulting performance parameters of the developed ASIC. It can be seen that there is an inverse correlation between the input referred noise density and the selected gain factor. The reason for this is the noise generated by the resistor in the output low-pass filter.

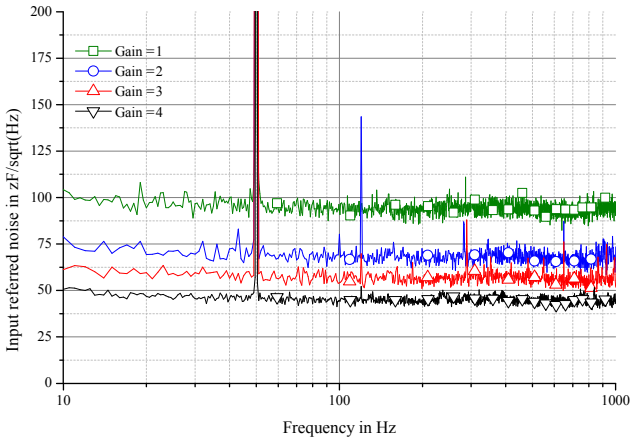


Figure 9. Measurement results of the input referred capacitance noise density.

For a low-gain setting, its influence is significant, while for high gain settings it becomes negligible.

For the highest gain setting a noise level below 50 zF/$\sqrt{\text{Hz}}$ was reached. As previously shown, the input referred noise is a function of the sensor's nominal and system's parasitic capacitance and thus could further be optimized for a specific sensing application. The dynamic range for each gain setting is given for a frequency range of 10 to 300 Hz.

6 Combination with a MEMS sensing element to a high-precision accelerometer

A high-sensitivity, low-noise MEMS sensing element has been developed by Mir Enterprises. A complete accelerometer system was built from the combination of the sensing element and the presented ROIC. Due to the very flexible design of the ROIC, there was no need for adaptations of the MEMS design to interface with the ASIC. The resulting acceleration measurement offers very high measurement accuracy and is well suited for high-precision applications as mentioned in Sect. 1.

The MEMS accelerometer sensing element is a typical capacitive device with in-plane, single-axis sensitivity fabricated in a SOI (silicon on insulator) process on an 8 inch wafer with a 50 µm structural layer. The principle of the fabrication process is described in detail in Sari et al. (2012); it relies on removing the handle wafer underneath the active device area by a process step in which the wafer is immersed in HF vapor. The HF vapor etches the silicon dioxide of the BOX (buried oxide layer) in areas where it can reach it; these are defined by two DRIE (deep reactive ion etching) steps performed first from the front and then from the back side. In this way the chips are separated without dicing and concurrently the handle wafer underneath the active area is freed, so that it can drop out in a controlled way. The yield of the fabrication process is very high, close to 100 %.

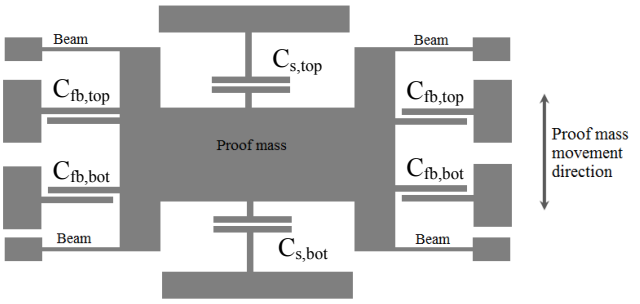


Figure 10. Block diagram of the MEMS sensing element.

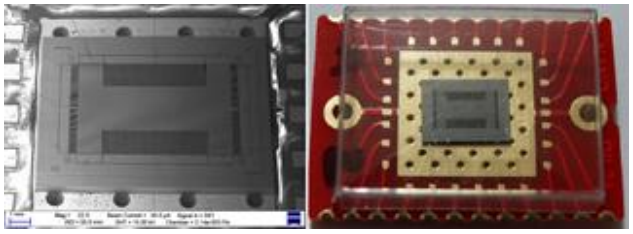


Figure 11. SEM image and photograph of the MEMS sensing element.

A block diagram of the sensing element is shown in Fig. 10. It has comb fingers on all sides of the H-shaped proof mass. The comb fingers on the left and right of the proof mass can be used for closed loop operation; however, these were not used in this work as only open loop tests were performed. The open loop comb fingers attached to the top and bottom of the proof mass form the sense capacitors with a nominal value of approximately 10 pF. The change in capacitance per 1 g ($= 9.81\,\text{m}\,\text{s}^{-2}$) is about $0.55\,\text{pF}\,\text{g}^{-1}$, which provides the input signal to the ASIC. The sensing element was packaged under atmosphere pressure. The main important parameters of the sensing element are summarized in Table 3. Figure 11 shows a scanning electron microscope (SEM) image of the chip (left) and a photograph of the chip mounted and wire-bonded on a carrier printed circuit board.

The noise floor of the sensor system, comprising the presented MEMS and developed readout ASIC, was measured on a vibration damped table and evaluated in the frequency range between 30 and 40 Hz, where environmental vibrations are absorbed most effectively. Figure 12 shows the measured acceleration equivalent noise (AEN) in a frequency range from 10 Hz to 1 kHz. An acoustic vibration source with a frequency of 180 Hz was placed in the measurement environment during measurement execution to ensure proper operation of the accelerometer. Peaks at this frequency and its odd harmonics can clearly be seen in the measured spectrum. A mean noise level of only 216 ng/$\sqrt{\text{Hz}}$ was measured in the specified frequency range. The noise level falls below 200 ng/$\sqrt{\text{Hz}}$ for certain frequencies. This is already close to the theoretical value of 136 ng/$\sqrt{\text{Hz}}$, which was calculated

Table 3. Parameters of the accelerometer.

Parameter	Value
MEMS sensing element	
Sensitivity	0.55 pF g^{-1}
Natural frequency	237 Hz
Overall device size	$7 \times 9 \times 0.6$ mm^3
Mass of proof mass	1.86 mg
Proof mass area	4×7 mm^2
Min. feature size	6 µm
Structural layer thickness	50 µm
BOX layer thickness	2 µm
Nominal capacitance	10 pF
Handle wafer thickness	525 µm
Brownian noise floor	100 ng/$\sqrt{\text{Hz}}$
Sensor and ROIC	
Sensitivity	0.7–2.67 V g^{-1} selectable
Measurement range	±5 g
Combined noise floor theoretical	136 ng/$\sqrt{\text{Hz}}$
Combined noise floor measured	216 ng/$\sqrt{\text{Hz}}$

using Eq. (13) for an electrical noise level of 46.75 zF/$\sqrt{\text{Hz}}$. The damping of the used table is nowhere perfect, which explains the remaining deviation from the theoretical value. Table 4 shows the performance values in comparison with other works. The full scale measurement range is more than ±5 g.

Significantly reduced noise levels are expected for further developments with vacuum sealed MEMS sensors. Reported systems that yield comparable performance to the one achieved in this work already take advantage of such a MEMS (Xu et al., 2015a, b).

7 Application in pressure sensing systems

At Fraunhofer IMS the fabrication of monolithically integrated surface micromachined pressure sensors has been established since 1994 (Dudaicevs et al., 1994). In this study sensing elements made of circular shaped, hermetically vacuum sealed, deflectable diaphragms for absolute pressure measurements were used. The sensing elements were produced in a 1.2 µm CMOS process on an 8 inch wafer. Details regarding fabrication and performance are given elsewhere (Trieu et al., 2002; Walk et al., 2015).

The sensors used in this study obtained arrays comprising pressure sensitive, deflectable as well as pressure insensitive, non-deflectable sensing elements, all with a nominal diameter of about 92 µm. The used sensor comprised 32 identical pressure sensing elements, which were electrically connected into an array. Additionally, another 32 pressure insensitive sensing elements were integrated, serving as reference capacitances. The overall 64 sensing elements were arranged

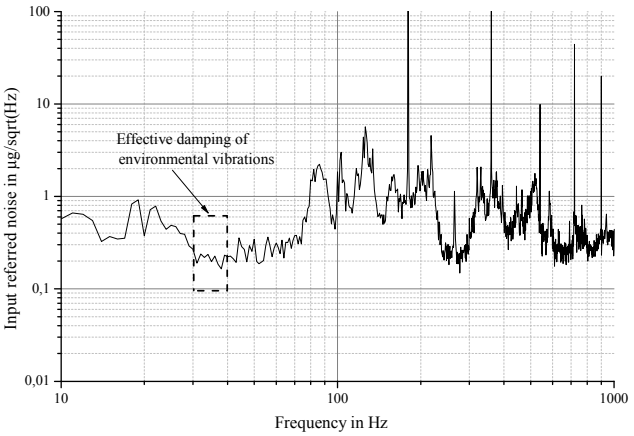


Figure 12. Measurement results of the input referred accelerometer noise.

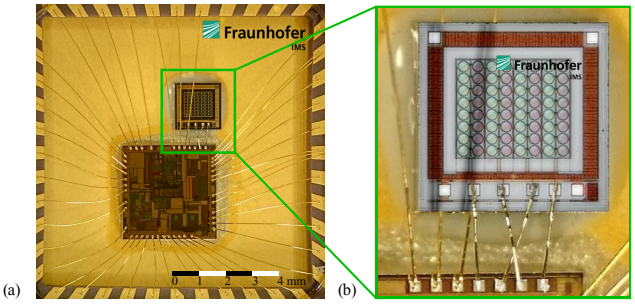


Figure 13. **(a)** Sensor system comprising the analog capacitive pressure sensor with sensing element diameters of about 92 µm and the C/V converting readout circuit, both mounted in a CLCC44 package. **(b)** Magnification of the pressure sensor.

in four electrically connected strings, each of eight sensitive and non-sensitive sensing elements. This circuitry was used to realize a sensor system as illustrated in Fig. 7d. The nominal capacitance of a string is approximately 16 pF.

The types of this family of capacitive pressure sensors show some cross-sensitivities. Due to the micro-mechanical structure, mechanical stress is also induced by different thermal expansion coefficients of the MEMS compared to the adhesive materials or the carrier housing materials (Gembaczka et al., 2014). Therefore, a soft silicone (Three Bond 1220H) is used as an adhesive for mechanically decoupling of the chip.

As shown in Fig. 13, the sensing element and ASIC were both mounted in a CLCC44 (ceramic leaded chip carrier) package, die-bonded by a very soft adhesive and wire-bonded by the use of Al wires (wedge–wedge bonds sensor to ASIC), and by the use of Au bonds (ball–wedge bonds to the package). No further glob top was applied. The package was sealed with a metal cover, which was equipped with a pressure port.

Table 4. Comparison with other systems.

Parameter	This work	Bernstein et al. (1999)	Wang et al. (2011)	Chen et al. (2014)	Yazdi et al. (2004)	Xu et al. (2015a)	Aaltonen and Halonen (2009)
Supply voltage in V	5	±10	1.8	±12	5	7 V	5 V
Noise floor in µg/$\sqrt{\text{Hz}}$	0.2	1.02	20.65	1.2	1.6	0.2	0.3
Bandwidth in Hz	10 k	1 k	100	500	95	300	300
Sensitivity in V pF^{-1}	3.0	1.26	0.3	0.95	1.6	1.9	2.5
Power dissipation in mW	300	–	0.036	–	12	23	77

The differential output voltage of the ROIC was measured using a Keithley™ 2000-20 digital multimeter (DMM) with an accuracy of better than 10 µV. The sensor system setup offered a SNR of about 120 dB regarding a full scale span (FSS) from −4 to +4 V at the system's output.

Figure 14 shows the system's outputs measured by the Keithley™ multimeter, whereas the temperature ranges from 0 to 80 °C in steps of 20 K with a maximum deviation of ±0.75 K. The presented results include an equidistant variation of the pressure from minimum to maximum values and then back to minimum again in 50 hPa steps. This measurement procedure was repeated twice for each temperature in order to investigate the repeatability and hysteresis behavior. Every data point represents the mean of 100 measurement values. At every pressure, a delay time of 30 s was used before 100 measurement results were recorded. The sensor system characteristics are shown over a span from 150 to 3000 hPa.

Here, two different operating conditions of the pressure sensor were employed: non-contact mode and contact mode, with a transition zone in between the two modes. In this zone a touch-down of the membrane to the substrate occurs. In contact mode operation, the membrane touches the substrate and the majority of the capacitance is due to the contact area of both electrodes (Pedersen et al., 2009). The increase in contact area is more linear along with pressure than in non-contact mode operation.

These measurements were executed at a minimum gain of the ROIC; thus, the differential, capacitive sensor signal correlates with a C/V conversion factor of 1.37 V pF^{-1}. In addition, an offset is applied by the aforementioned internal trimming capacitances C_{trim} (see Fig. 1) to align the differential output signal.

The aforementioned cross-sensitivities become clear in terms of a temperature dependency of about 0.35 V K^{-1}. This indicates that an accurate temperature measurement improves the measurement accuracy of capacitive pressure sensor systems.

Moreover, the hysteresis of up to a few parts per thousand is mainly due to a temperature mismatch of the die bond materials regarding the sensor die. Further, pressure is also known to affect the die bond.

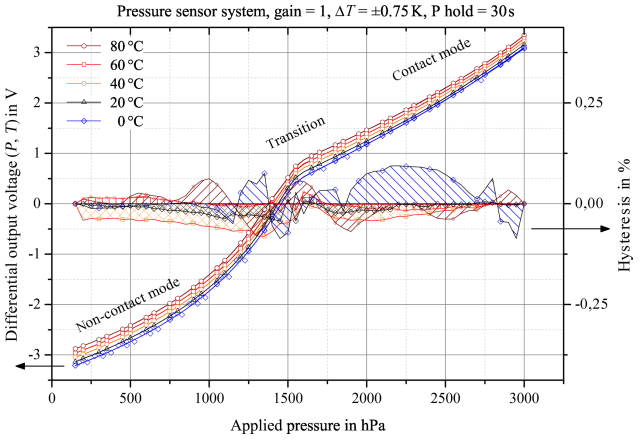


Figure 14. Exemplary output curves and hysteresis are plotted against applied pressure within a temperature span of 0 to 80 °C, within a full scale range of the applied pressure of 150 to 3000 hPa.

The plots in Fig. 14 obtain 1σ errors of some tens of µV, which are predominately given by external impacts on the sensor system, such as by the pressure regulatory mechanisms of up to ±0.5 hPa, uncompensated temperature deviations of up to ±0.75 K for each temperature and pressure leakage rates of magnitudes of 1 to 7 Pa s^{-1}. These effects caused limitations to the SNRs for the FSS from 150 to 3000 hPa regarding the maximum differential output voltage range of about 6 V absolute. A limitation of the SNRs to about 95 dB at about 80 °C was observed. For lower temperatures the SNR increases to about 105 dB.

According to Table 2, the calculated SNRs are close to the dynamic range of 124–130 dB of the ROIC presented before. As presented in Fig. 15, the overall system performance yields a noise floor of approximately 42 mPa/$\sqrt{\text{Hz}}$ and lower. The presented noise floor was measured at atmospheric pressure in a laboratory environment without mechanical damping to the surrounding. For pressure sensor applications, low frequencies were involved. Thus, the SNR can be obtained by integration from 10 to 50 Hz.

For the data shown in Fig. 15, a SNR of about 101 dB can be calculated. This is in very good agreement with SNRs of

Table 5. Parameters of the pressure sensor.

Parameter	Value
Pressure sensing element	
Sensitivity (non-contact mode)	$\sim 1.8\,\mathrm{fF\,hPa^{-1}}$
Sensitivity (contact mode)	$\sim 1.2\,\mathrm{fF\,hPa^{-1}}$
Overall device size	$1.8 \times 1.8 \times 0.7\,\mathrm{mm^3}$
Diaphragm diameter	92 µm
Diaphragm height	1.1 µm
Mass of a single diaphragm	15.5 ng
Min. feature size	1.2 µm
Cavity height	0.7 µm
Nominal capacitance	16 pF
Brownian noise floor at 0.1MPa	$50\,\mathrm{nPa}/\sqrt{\mathrm{Hz}}$
Sensor and ROIC	
Sensitivity	$25\text{–}100\,\mu\mathrm{V\,Pa^{-1}}$ depending on FSS and gain
Measurement range	150–3000 hPa
Combined noise floor theoretical	$5.5\,\mathrm{mPa}/\sqrt{\mathrm{Hz}}$
Combined noise floor measured	$42\,\mathrm{mPa}/\sqrt{\mathrm{Hz}}$ at 10 Hz

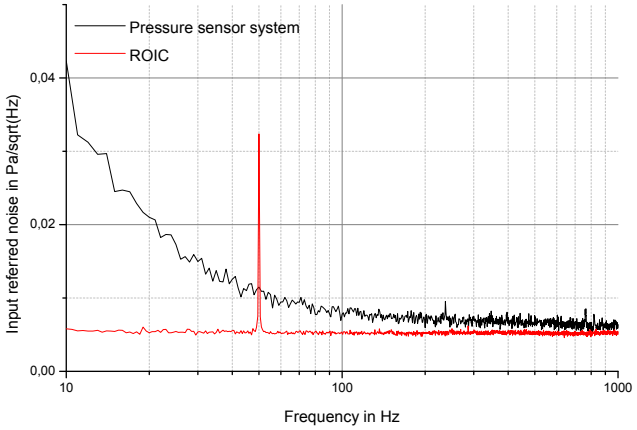


Figure 15. Measurement results of the input referred pressure noise at room temperature and atmospheric pressure, compared to the input referred noise of the ROIC alone.

105 dB calculated by the applied FSSs over the measured 1σ errors.

For low frequencies, the impact of an input pressure noise p_n due to Brownian motion on single, ideal capacitive diaphragms can be calculated by

$$\overline{p_n^2} = 1.15 \cdot \sqrt{32 \cdot \frac{k_B T}{\pi}} \cdot \frac{\left(\sqrt{m_1}p_1 + \sqrt{m_2}p_2\right)\mathrm{BW}}{a^2}, \qquad (15)$$

where m_1, m_2 are the masses of the gas molecules and p_1, p_2 are the mean gas pressures on both sides of the diaphragm, BW the bandwidth and a the diaphragm's radius (Chau and Wise, 1987).

To numerically calculate the Brownian noise per unit bandwidth of a single diaphragm surrounded by air, the following parameters are used: $m_1 = m_2 = 4.78 \times 10^{-26}$ kg, $T = 300$ K, $p_1 = 1$ Pa, $p_2 = 0.1$ MPa, and $2 \cdot a = 92$ µm. According to Eq. (15), the rms (root mean square) noise due to Brownian motion is of a magnitude of about $50\,\mathrm{nPa}/\sqrt{\mathrm{Hz}}$, and thus is negligible compared to the measured noise presented in Fig. 15.

The measured noise floor in the low frequencies is by a factor of 8 higher than the combined theoretical noise floor of the ROIC. A possible explanation for the higher measured noise floor could be either due to environmental surroundings or due to well-known high built-in stresses in the diaphragms (Trieu et al., 2002; Chau and Wise, 1987).

The main parameters of the pressure sensing element are summarized in Table 5.

An analog capacitive pressure sensor was characterized by the aid of the introduced ultra-low noise differential interface ASIC. The obtained sensor system will enable further investigations and technological advancements. For example, the system can be used to accurately evaluate mechanical hysteresis in high dynamics. These and other issues can be characterized effectively in detail due to a very high SNR.

Furthermore, the characterization of impacts on the mechanical noise floor will help to drive the continuous development of this sensor technology to develop highly accurate pressure sensors, for example for very low-pressure metering.

8 Conclusion and outlook

The architecture of an analog, fully differential readout circuit for capacitive sensors such as pressure sensors or an accelerometer MEMS was presented in this paper. The main design goal was low noise and hence high measurement accuracy. Special emphasis was put on the design of the amplifiers in the C/V conversion stage. The resulting ROIC has a noise floor of less than 50 zF/$\sqrt{\text{Hz}}$ in combination with a large measurement range of up to ±3 pF, which leads to a very high dynamic range of 124–130 dB, depending on the selected conversion gain.

An accelerometer was presented which comprises the low-noise ROIC and a high-sensitivity, low-noise sensing MEMS sensing element. The overall system performance yields a noise floor of only 200 ng/$\sqrt{\text{Hz}}$.

The developed ASIC was combined with a CMOS integrated pressure sensor. The sensor system provides a very high SNR of more than 105 dB, which allows high-precision measurements and further technological advances in the pressure sensor process.

Future trends in the use of MEMS based sensors require operation in harsh environments where operation under high temperature, insensitivity against shocks (e.g., accelerations up to 20 000 g in guided ammunition, "gun-hard") or resistance against aggressive chemical media or radiation is essential. Further examples of such applications are downhole drilling in oil and gas production or sensors for aerospace (Stauffer, 2006).

The presented ROIC and sensor system designs show strong potential for such applications. The developed IC is capable of operating at very high temperatures of up to 170 °C. For even higher temperatures exceeding 250 °C, Fraunhofer IMS offers an SOI CMOS technology. A transfer of the IC design to that technology would enable use for very high temperatures. Bulk micromachined accelerometer sensing elements like the one presented in this work are already known to be robust against very high accelerations and repetitive shocks (Stauffer et al., 2010). Future investigations would target mounting and assembly technologies. For MEMS-CMOS integration flip-chip bonding by high-temperature solid–liquid interdiffusion (HT-SLID) technology is available. For adequate protection against chemically aggressive media in combination with high temperatures, layers based on atomic layer deposition (ALD) have been developed.

The application of those technologies for the development of robust and reliable MEMS based sensor systems as well as their characterization will be the subject of future research activities.

Biographies

A. Utz received a Dipl.-Ing. degree in electrical engineering and electronics from the University of Dortmund, Germany, in 2005 and a Dr.-Ing. degree from the University of Duisburg, Germany, in electrical engineering in 2012.

From 2006 to 2008 he worked as a R & D engineer at Plastcontrol GmbH, a company which develops control systems for industrial process automation. Since 2008 he has been with Fraunhofer IMS, first gaining his Dr.-Ing. degree, and afterwards till now as a research associate in the field of mixed signal IC design.

C. Walk received B.Sc. and M.Sc. degrees from the University of Freiburg, Germany, in 2009 and 2012, respectively. He studied microsystems engineering at the University of Freiburg with a focus on optics and process technologies.

In 2012 he was a research assistant at the Fraunhofer Institute for Solar Energy Systems (ISE), Freiburg, working in the field of optics and micro- and nano-structured functional surfaces. Since 2012 he has been with Fraunhofer IMS. From 2012 until 2014 he was a research assistant and since 2014 he has been working as a PhD student in the field of post-CMOS sensor development.

N. Haas received his Dipl.-Ing. degree from the University of Duisburg, Germany, in electrical engineering with a focus on microelectronics in 1999.

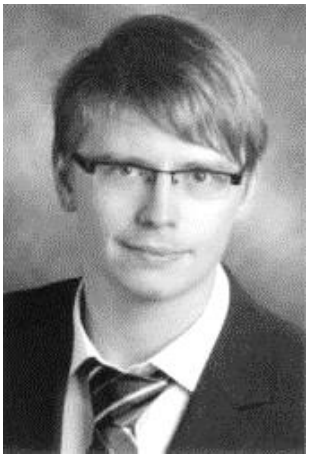
Since 1999 he has been with Fraunhofer IMS as a scientific assistant, business unit IC design and ASICs.

T. Fedtschenko received a Dipl.-Ing. degree from the National Technical University in Kharkiv, Ukraine, in 1989. She studied physics and technology engineering with a focus on high-voltage electrical engineering.

Since 2001 she has been scientific assistant with Fraunhofer IMS, business unit IC Design and ASICs.

M. Görtz received his diploma from Niederrhein University of Applied Sciences in 2001 in electrical engineering, with a focus on electrical/optical communication and the production technologies of microsystems.

From 2001 to 2004 he was at Fraunhofer IMS to design and test neuronal vision prostheses with microsystem technologies. Between January 2004 and February 2005 he was at the Institute of Materials in Electrical Engineering 1 at RWTH Aachen University working on active implantable medical devices. Since March 2005 he has been back at Fraunhofer IMS and is responsible for development of medical implants. Currently he is group manager and head of the Pressure Sensor Systems business field.



A. Stanitzki received a diploma degree in electrical engineering from Ruhr-University Bochum in 2008.

From 2007 to 20011 he worked at advICo microelectronics GmbH as an IC design engineer for RF-mixed-signal and radhard applications. Since 2012 he has led the Mixed Signal IC Design group within Fraunhofer IMS, with a focus on energy harvesting medical implants, industrial precision sensor readout ICs and functional safety in analog ICs.

M. Mokhtari received a BEng degree in electronics engineering from the University of Southampton, UK, in 2000 and a PhD degree in microelectronics from the University of Southampton, UK, in 2004, with a focus on oversampling sigma-delta modulators for advanced MEMS inertial sensors.

From 2004 to 2007 he worked as the Research Business Manager at Innos Ltd, UK, developing and manufacturing rollable display technologies. He founded Mir Enterprises Ltd, UK, in 2007 and has held the position of Managing Director to date. The company specializes in the design, fabrication and testing of micro and nano device technologies in both research and low-volume manufacturing. He was appointed as a member of the advisory board at the London Technology Network from 2009 to 2010.

M. Kraft currently is a Professor of Micro- and Nanosystems at the University of Liege, Department of Electrical Engineering and Computer Science (Montefiore Institute). From 2012 to 2014 he was at Fraunhofer IMS in Duisburg, Germany, where he headed the Department of Micro- and Nanosystems, focussing on fully integrated microsensors and biohybrid systems. He concurrently held the W3 Professorial Chair of Integrated Micro- and Nanosystems at the University of Duisburg-Essen.

From 1999 to 2012 he was a faculty member and Professor of Micro-System-Technology at the University of Southampton, UK. He graduated with a Dipl.-Ing. (Univ.) in electrical and electronics engineering at Friedrich Alexander Universität Erlangen-Nürnberg in 1993. In 1997 he was awarded a PhD from Coventry University, UK, on the development of a MEMS accelerometer. He then spent 2 years at the Berkeley Sensors and Actuator Center at the University of California, working on integrated MEMS gyroscopes.

R. Kokozinski received a Dipl.-Ing. degree in electrical engineering in 1990 and a Dr.-Ing. degree in 1996, both from the University of Duisburg, Germany.

In 1990 he joined the Signal Processing and System Design Department at Fraunhofer IMS, working in the area of analog and mixed analog–digital CMOS and BiCMOS IC design. From 1998 to 1999 he was with Toshiba Electronics Europe, Düsseldorf, Germany, where he headed the development of high-speed CMOS interface cells as well as the development of mixed-signal telecommunication ICs, e.g., for xDSL applications. He is now a Professor at the University of Duisburg-Essen, Duisburg, Germany, and Head of the Integrated Circuits and Systems Department at Fraunhofer IMS. His research interests include design of microelectronic circuits and systems, analog and digital signal processing as well as design techniques for medical implants, functional safety, harsh environments and high-temperature electronics.

Data availability. No data sets were used in this article. Raw data of the presented measurements are available upon request to the author.

Competing interests. The authors declare that they have no conflict of interest.

Author contributions. AU, AS, NH, TF and RK designed the presented ASIC. MM and MK developed the accelerometer sensing MEMS, CW and MG the pressure sensor IC. The combination of ROIC and sensing elements into both pressure and acceleration sensing systems was performed by CW. Measurement setups were developed and measurements performed by CW and AU. AU and CW prepared the manuscript with contributions from all co-authors.

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